Preliminary

Specification of

YACG4C0C9SHC

[Rev. 0.1]

1/4” 8M Pixel

CMOS Image Sensor

[Hi-843]

This document is a general product description and is subject to change without notice. Check for latest version of this document, contact to SK hynix FAE(cis_ae@skhynix.com). SK Hynix does not assume any responsibility for use of circuits described. No patent licenses are implied.

Revision History

Version	Date	Comments
0.0	2015/04/28	YACG4C0C95HC Datasheet is released(Preliminary)
0.1	2015/6/30	Table of power consumption is updated Spectral Response data is updated.

Disclaimer
This document is subjected to change without notice to customers.
Check for lateset version of this document, contact to SK hynix FAE(cis_ae@skhynix.com).

General Precautions
Do not disclose the document to third parties without prior permission from SK Hynix Inc.

Contents

Figure Contents

Table Contents

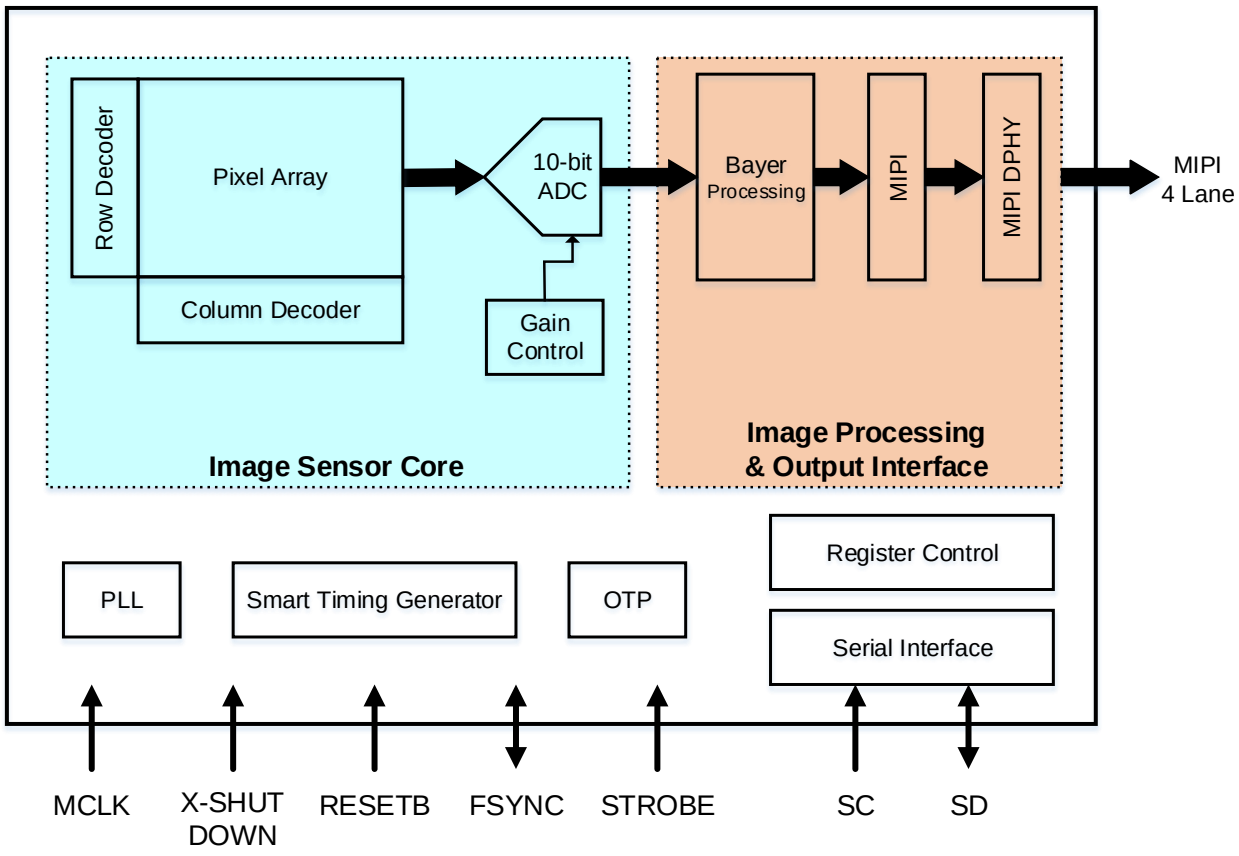
1. OVERVIEW

1.1. Description

YACG4C0C95HC is a high quality 8mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.

YACG4C0C9SHC incorporates a 3280 x 2464 pixel array, on-chip 10-bit ADC and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise and random noise.

<Figure 1. Block Diagram>



1.2. Applications

- Mobile Phone Camera / Digital Still Camera
- PC Camera / Video Conference

1.3. Key Features

- Pixel Size : 1.12um X 1.12um, BSI
- Effective Image Size : 3673.60um (H) X 2759.68um(V)
- Resolution : 3,264H X 2,448V
- Color Filter : RGB Bayer
- Optical Format : 1/4 inch
- Frame Rate : 30fps@ QUXGA, 60fps@ Full HD 1080P(Crop), 90fps@ HD 720P
- Power Supply :
  Analog : 2.8V,
  IO : 1.8V / 2.8V
  Core(Digital) : 1.2V
- Power Consumption :
  168mW@ 30fps, QUXGA
  150mW @ 60fps, FHD 1080P(Crop)
  150mW @ 90fps, HD 720P
- ADC : 10bit
- PLL : On Chip
- Operation Temperature: -20 ~ 60°C
- Master Clock : 6 ~ 27MHz
- Output Format : RGB Bayer 10
- Windowing : Programmable
- Host Interface : two-wire serial bus interface
- Sub-Sample : 1/2, 1/4
- Image Flip : X/Y Flip
- Black Level Calibration
- Digital gain control : x1 ~ x16, (1/512 step)
- Built-in test pattern generation
- Internal PLL for high speed clock generation
- MIPI 4-Lane (Max 720Mbps on each lane)
- Standby mode for power saving
- OTP 8KB
- 1D Lens Shading Correction
- Strobe Control : Support Xenon / LED Type
- On-chip Defect correction for couplets & Clusters
- Line-interlaced long-short output for HDR

2. Electrical characteristics

2.1. Key Features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	$V_{DD:D}$	1.1	1.2	1.3	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.6	2.8	3.0	V	
Analog Pixel Circuit Power Supply Voltage	$V_{DD:P}$	2.6	2.8	3.0	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7	1.8/2.8	3.0	V	
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	

[Table 2. AC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
MCLK	Frequency	6		27	MHz	
MCLK	Duty Cycle	45	50	55	%	
MCLK	Rise/Fall time			4	ns	
SC	Frequency	100		400	KHz	

[Table 3. Temperature Characteristics]

Item	Symbol	Rating	Unit	Note
Storage Temperature	T_{STR}	-40 ~ 80	°C	
Functional Operating Temperature	T_{FUN}	-20 ~ 60	°C	Camera fully functional

[Table 4. Power Consumption]

Case1) MIPI interface

Item	Condition		Min	Typ	Max	Unit	Note
Full@30fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			30	36	mA	1
	$V_{DD:D}$=1.2V			68	82	mA	
	$V_{DD:I}$	1.8V		1	2	mA	2
		2.8V		1	2	mA	
FHD 1080P@60fps (Crop)	$V_{DD:A}$ &$V_{DD:P}$=2.8V			30	36	mA	1
	$V_{DD:D}$=1.2V			53	64	mA	
	$V_{DD:I}$	1.8V		1	2	mA	2
		2.8V		1	2	mA	
HD 720P@90fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			30	36	mA	1
	$V_{DD:D}$=1.2V			53	64	mA	
	$V_{DD:I}$	1.8V		1	2	mA	2
		2.8V		1.5	2	mA	
Stand by Current					200	uA	3

Note1) Because current of analog circuit depends on the registers' values, it is measured at specific register's value .
Note2) Because power consumption of VDD:I depends on the output load and system environment, users should supply enough current to sensor for stable operation. It is measured when output load is floated.
Note3) Standby current is measured at XSHUTDOWN = LO and MCLK = LO.
We recommend that power should be turned off, when low standby power consumption is required

2.2. MIPI Features

[Table 5. HS Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|△VCMTX(1,0) |	VCMTX mismatch when Differential-1 or Differential-0			5	mV
| VOD |	HS transmit differential voltage	140	200	270	mV
|△VOD |	VOD mismatch when Differential-1 or Differential-0			10	mV
VOHHS	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
△ZOS	Single ended output impedance mismatch			10	%

[Table 6. HS Transmitter AC Specifications]

Parameter	Description	Min	Typ	Max	Unit
△VCMTX(HF)	Common-level variation above 450MHz			15	mVRMS
△VCMTX(LF)	Common-level variations between 50-450MHz			25	mVPEAK
tR and tF	20% ~ 80% rise time and fall time			0.3	UI
		150			ps

[Table 7. LP Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VOH	Thevenin output high level	1.1	1.2	1.3	V
VOL	Thevenin output low level	-50		50	mV
ZOLP	Output impedance of LP transmitter	110			Ω

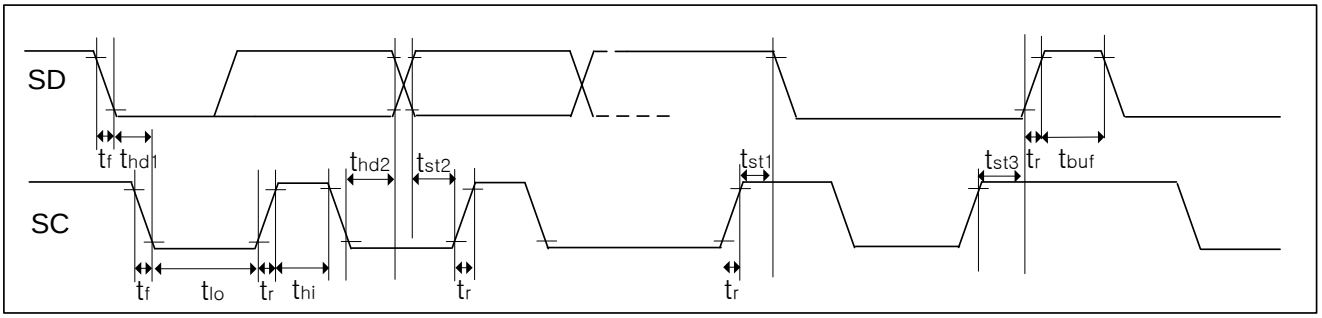
[Table 8. LP Transmitter AC Specifications]

Parameter	Description		Min	Typ	Max	Unit
TRLP/TFLP	15%~85% rise time and fall time				25	ns
TREOT	30%~85% rise time and fall time				35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive – OR clock	First LP exclusive – OR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
TLP-PER-TX	Period of the LP LP exclusive – OR clock		90			ns
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns
	Slew rate @ CLOAD = 20pF		30		150	mV/ns
	Slew rate @ CLOAD =70pF		30		100	mV/ns
CLOAD	Load capacitance		0		70	pF

3. Two-Wire Serial Bus Interface

3.1. Timing Specifications

<Figure 2. AC Timing of Two Wire Serial Bus >



[Table 9. AC Characteristics of Two Wire Serial Bus]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SC frequency	f_{sck}			400	KHz
SC low period	t_{lo}	1.2		-	us
SC high period	t_{hi}	0.6		-	us
SC setup time for START condition	t_{st1}	0.6		-	us
SC setup time for STOP condition	t_{st3}	0.6		-	us
SC hold time for START condition	t_{hd1}	0.6		-	us
SD setup time	t_{st2}	0.6		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	0.6		-	us
Rising time of both SD and SC	t_r	-		0.3	us
Falling time of both SD and SC	t_f	-		0.3	us
Capacitive load of SC/SD	C_b	-		100	pF
Pull-up resistor on SC and SD			1.5		kΩ

3.2. Bus Operation

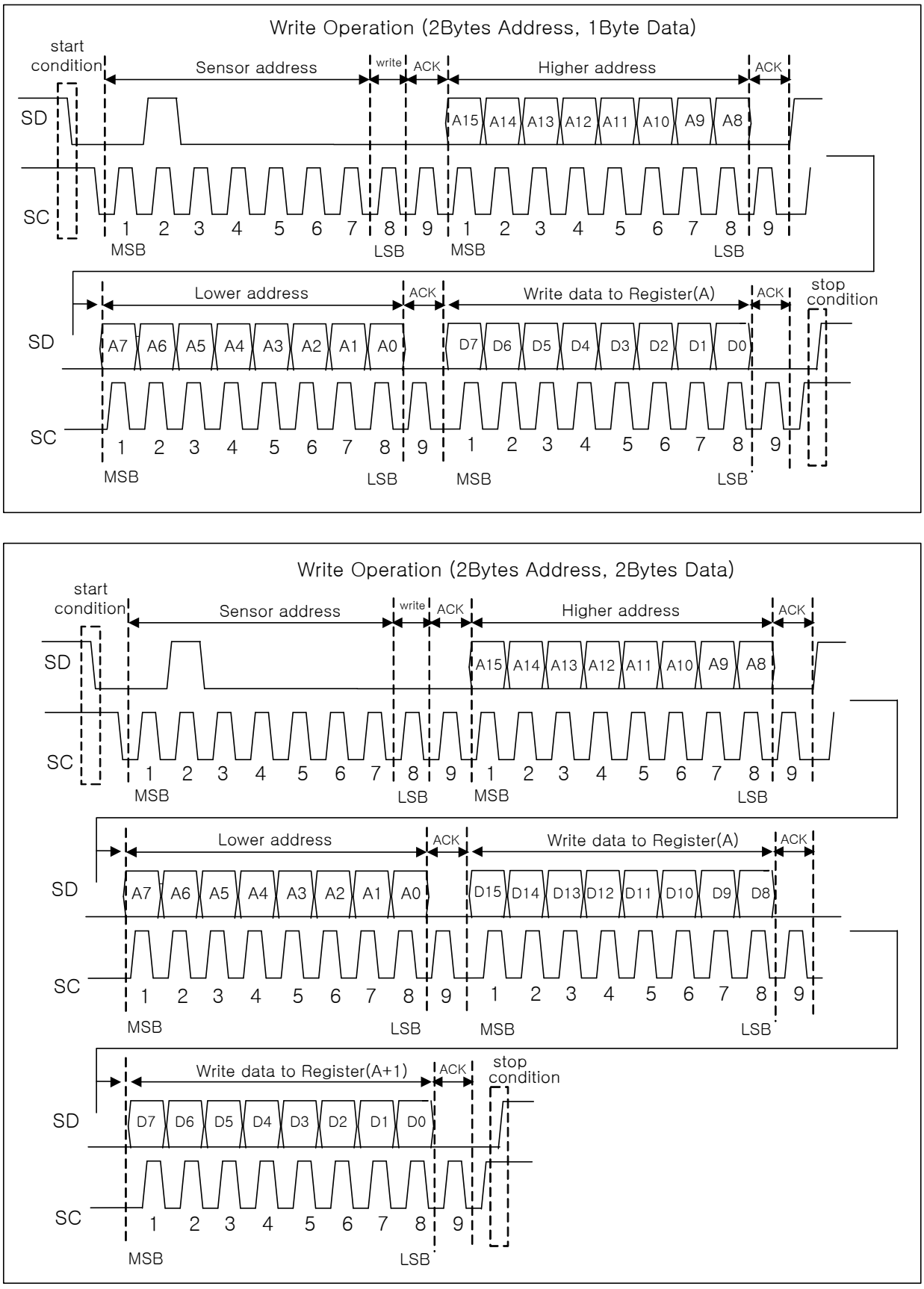
The two-wire serial bus interface is used to write and read the required data into registers in this sensor. Sensor can operate as a slave device only. The two-wire serial bus interface is controlled by SD (serial data) and SC (serial clock). SD is bidirectional bus.

Operation has single byte programming and multiple byte programming. Users doesn't need to set continuously register address on programming multiple byte because the sensor increases register address automatically. This will reduce time to program registers.

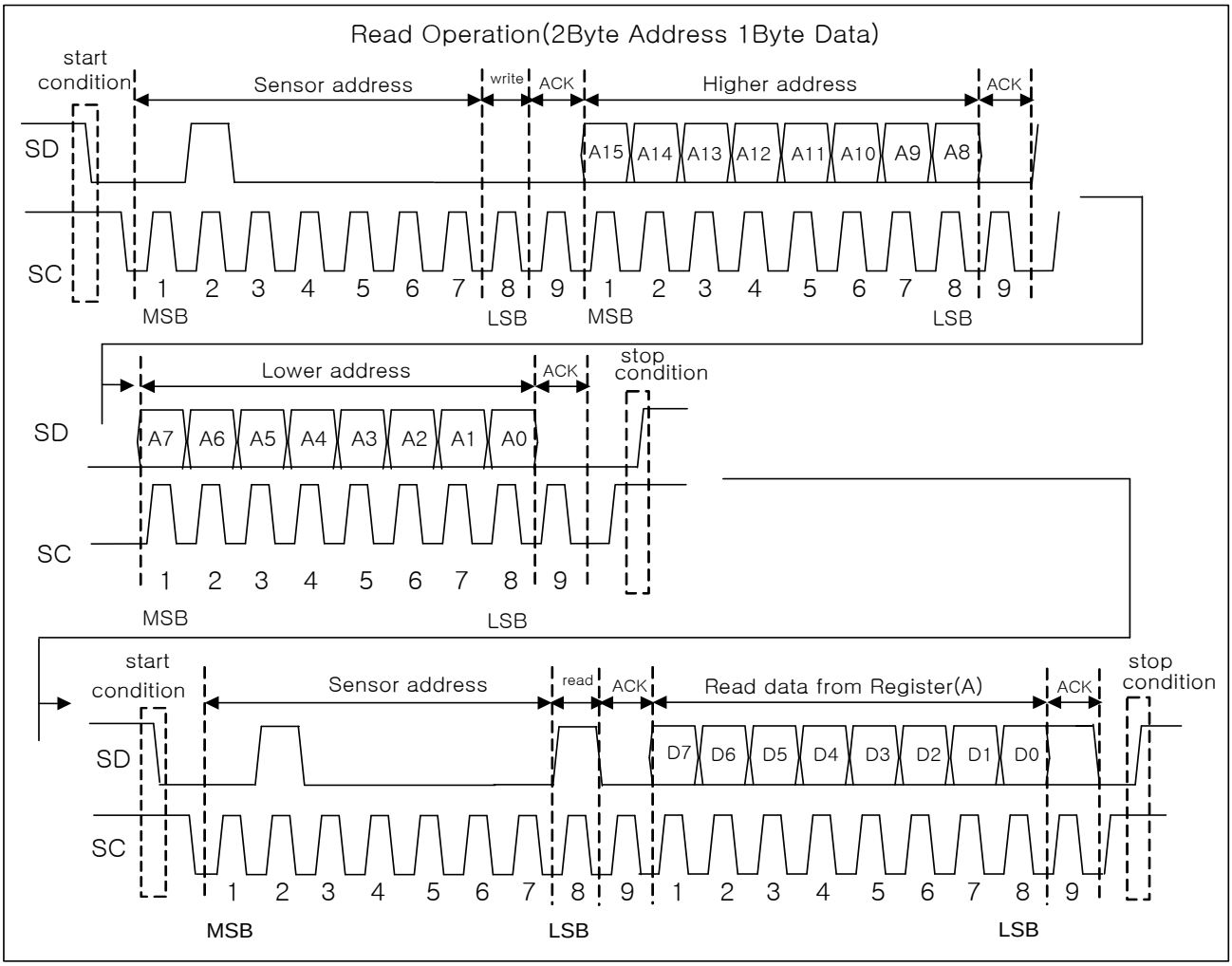
Following figures show write and read operations.

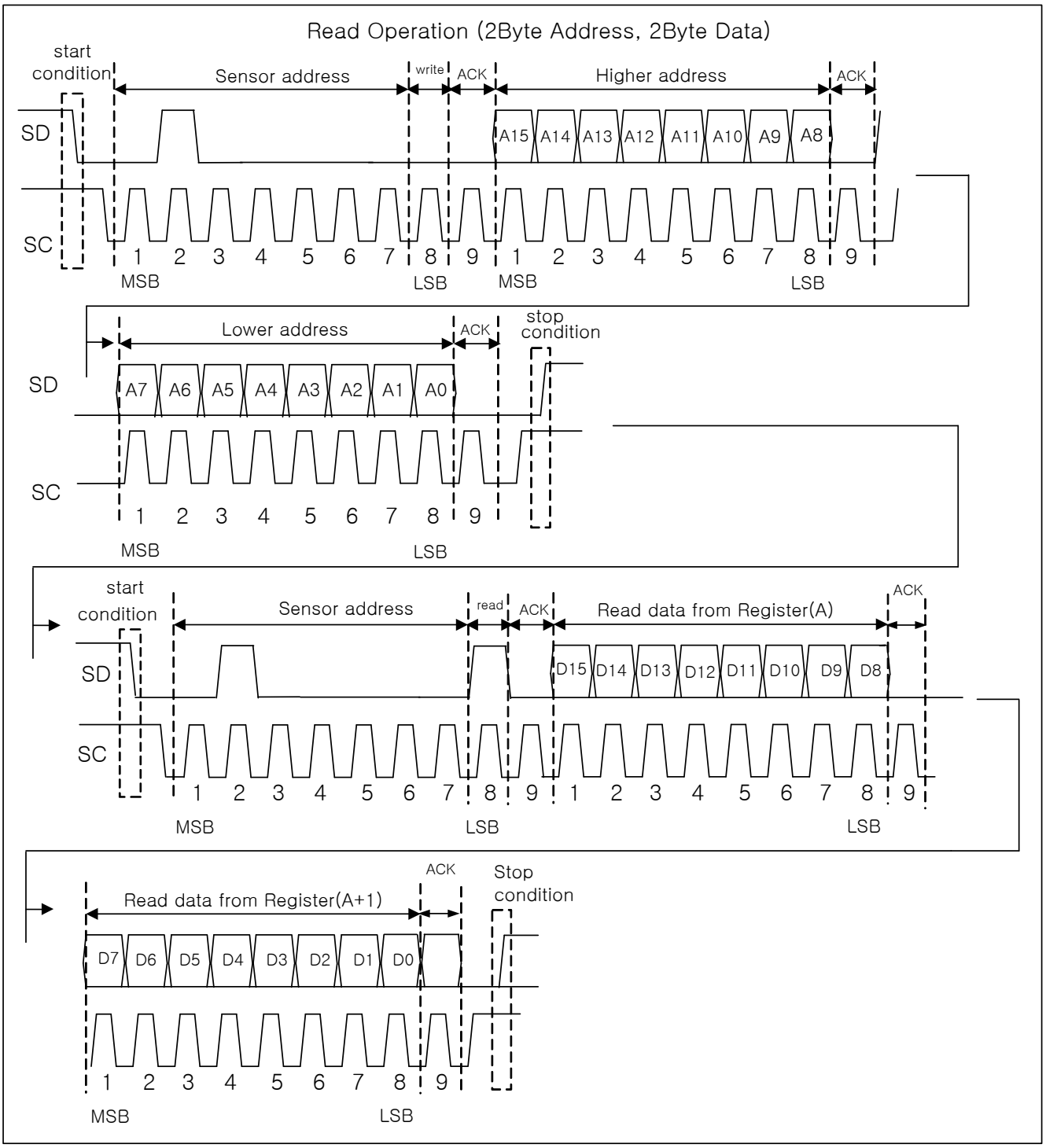
Note) Before programming the two-wire serial bus interface, MCLK and RESETB should be supplied..

<Figure 3. Write Operation through Two Wire Serial Bus >



<Figure 4. Read Operation through Two Wire Serial Bus >

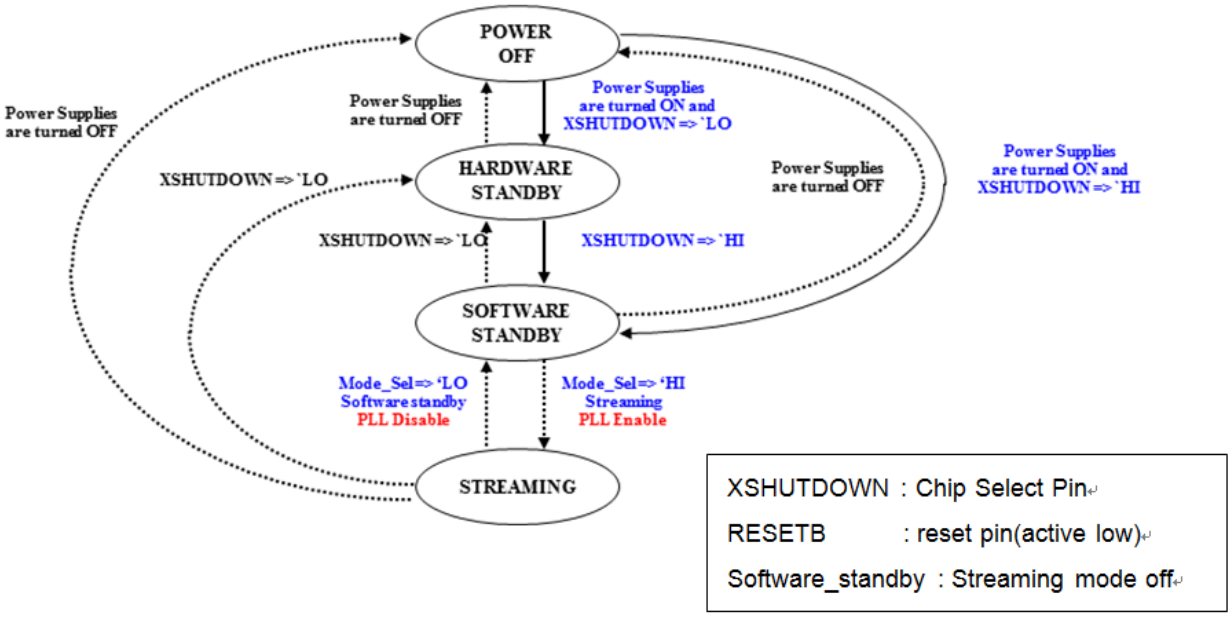



Read Operation (2Byte Address, 2Byte Data)
start condition
Sensor address
write
ACK
Higher address
ACK
SD
A15 A14 A13 A12 A11 A10 A9 A8
SC
1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9
MSB
LSB
MSB
LSB
Lower address
ACK
stop condition
SD
A7 A6 A5 A4 A3 A2 A1 A0
SC
1 2 3 4 5 6 7 8 9
MSB
LSB
start condition
Sensor address
read
ACK
Read data from Register(A)
ACK
SD
D15 D14 D13 D12 D11 D10 D9 D8
SC
1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9
MSB
LSB
LSB
ACK
Stop condition
Read data from Register(A+1)
D7 D6 D5 D4 D3 D2 D1 D0
1 2 3 4 5 6 7 8 9
MSB
LSB

4. FUNCTION DESCRIPTION

4.1. Operation Mode

<Figure 5. System State Diagram>



[Table 10. Operation Mode Summary]

Power State	Description	Activate	Power
Power OFF	Power supplies are turned off	None	0uA
Hardware Standby	No communication with the sensor is possible Low level on XSHUTDOWN pin or stopping EXTCLK	XSHUTDOWN Low	200uA
Software Standby	CCI communication with sensor is possible PLL is ready for fast return to Streaming mode	Power consumption is arrowed to achieve fast transition between streaming and SW Standby modes. MCLK Pad Enabled	6mW
Streaming	The sensor module is fully powered and is streaming image data on the CCP2 bus. (Initialized all logic block with APOR)	All Logic, MCLK Pad Enabled	160mW

In operating mode, two type of usage may be possible.

First, XSHUTDOWN and RESETB pin is used to control the operating mode which is traditional way.

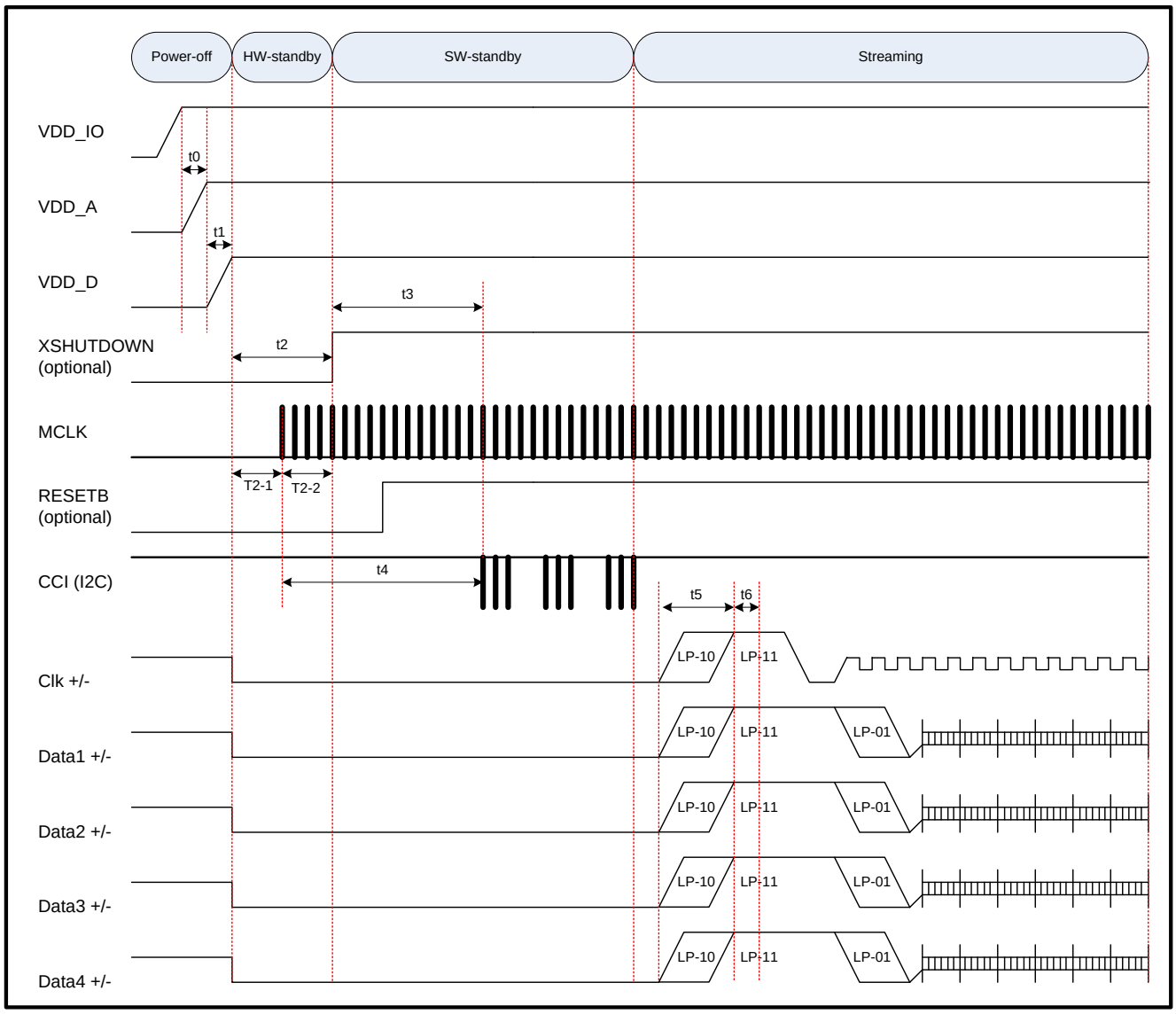
Second, to minimize the module pin connection, XSHUTDOWN and RESETB can be omitted in module connection. In the case, the sensor will be automatically enabled when external clock(MCLK) is active. And then, the internal POR is used to initialize the sensor status.

4.2. Power Timing

Power On Sequence

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.2V (ON) → MCLK(ON) → XSHUTDOWN(L→H) → RESETB(ON) → Set registers for normal operation → Normal Operation

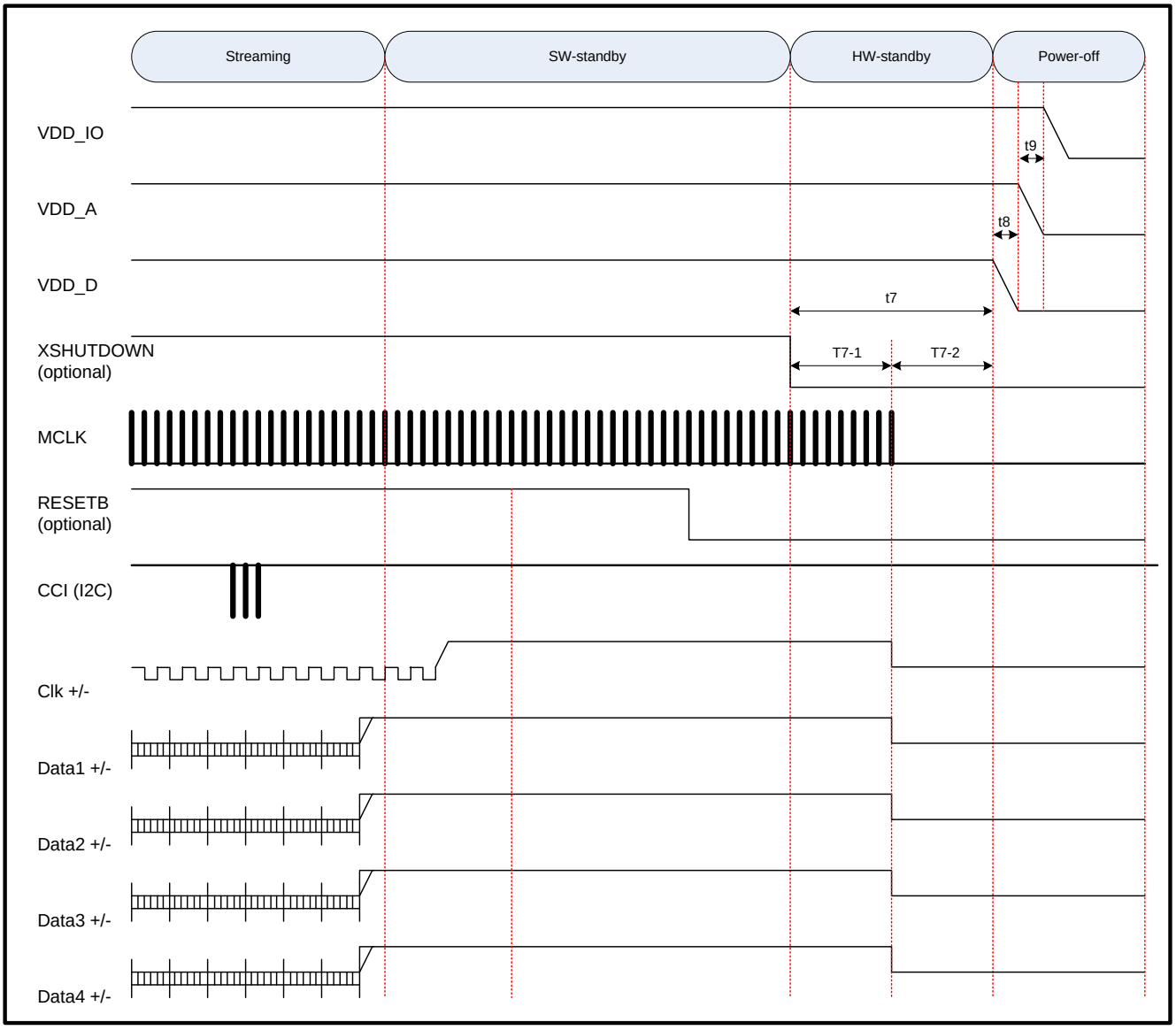
<Figure 6. Timing of Power on Sequence>



Power Off Sequence

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → XSHUTDOWN(H→L)→ MCLK(OFF)→ VDDD 1.2V (OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

<Figure 7. Timing of Power off Sequence>



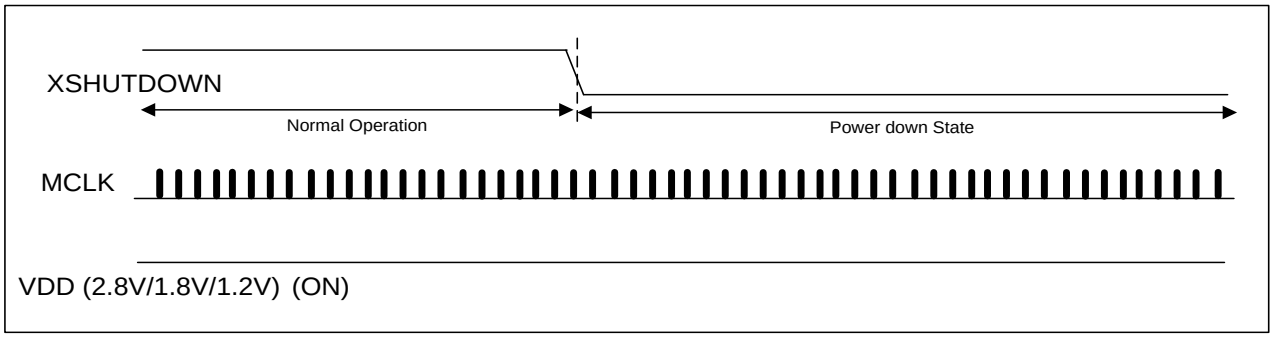
[Table 11. Timing of Power Sequence]

Constraint	Label	Min	Max	Unit
VDD_IO rising – VDD_A rising	t_0	VDD_IO, VDD_A and VDDD may rise in any order The rising separation can vary from 0ns to indefinite		ns
VDD_A rising – VDD_D rising	t_1			ns
VDD_D rising – XSHUTDOWN rising	t_2	0.0		ns
VDD_D rising – MCLK running	t_{2-1}	0.0		ns
MCLK running – XSHUTDOWN rising	t_{2-2}	0.0		ns
XSHUTDOWN rising – First I2C transaction	t_3	2400		MCLK cycles
Minimum no of EXTCLK cycles prior to the first I2C transaction. With XSHUTDOWN.	t_4	2400		MCLK cycles
D-PHY power-up	t_5	1	1.1	ms
D-PHY init	t_6	100	110	us
XSHUTDOWN falling – VDD_D falling	t_7	0.0		ns
XSHUTDOWN falling – MCLK stop	t_{7-1}	0.0		ns
MCLK stop – VDD_D falling	t_{7-2}	0.0		ns
VDD_D falling – VDD_A falling	t_8	VDD_IO, VDD_A and VDD_D may fall in any order. The falling separation can vary from 0ns to indefinite		ns
VDD_A falling – VDD_IO falling	t_9			

From Normal Operation State to Stand-by(Power down) State

When XSHUTDOWN is disabled, output pins go to Hi-Z.

<Figure 8. Timing of Normal to Stand-by>



From Stand-by(Power down) State to Normal Operation State

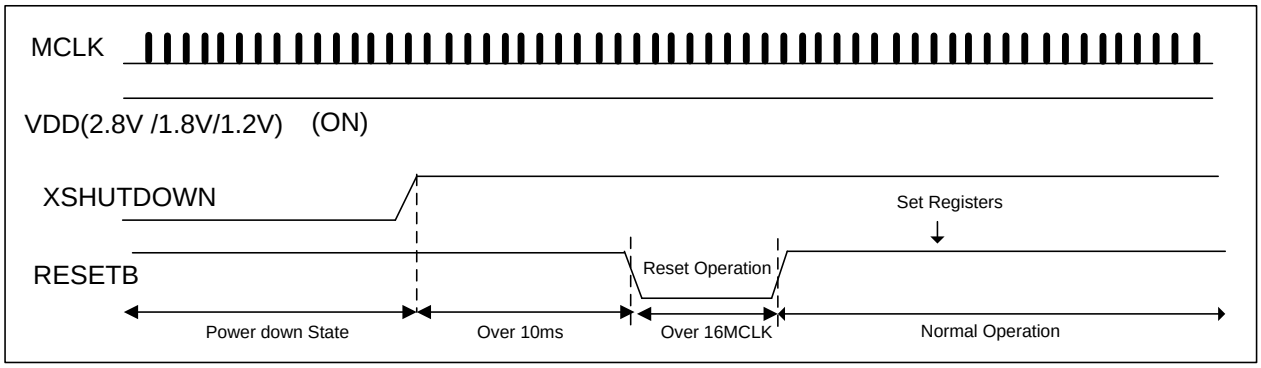
1) Set XSHUTDOWN to Hi.

2) Wait 10ms.

3) Set RESETB from Low to Hi.

4) Set the registers for normal operation

<Figure 9. Timing of Stand-by to Normal >



4.3. Black Level Calibration(BLC)

Black level is caused from pixel characteristics and analog channel offset. It makes poor image quality in dark condition and misleads color balance. To reduce these phenomenon, sensor automatically calibrates the black level every frame. The masked pixels in pixel array are used to calculate the black level.

4.4. Analog Gain Control

Global gain register (0x003B) sets the analog gain. The maximum analog gain is 16x. Below Table shows the recommended gain settings:

Addr.	Register Name	Description	Default
0x003B	analog_gain_code_global	Analog Gain *register value range = 0x00 ~ 0xF0(recommend)* $\text{Analog Gain} = \frac{Reg.value}{16} + 1$	0x00

[Table 12. Analog Gain Setting]

Register value		Gain(X)	Register value		Gain(X)
Dec	Hex		Dec	Hex	
0	0x00	x1.0	128	0x80	x9.0
8	0x08	x1.5	136	0x88	x9.5
16	0x10	x2.0	144	0x90	x10.0
24	0x18	x2.5	152	0x98	x10.5
32	0x20	x3.0	160	0xA0	x11.0
40	0x28	x3.5	168	0xA8	x11.5
48	0x30	x4.0	176	0xB0	x12.0
56	0x38	x4.5	184	0xB8	x12.5
64	0x40	x5.0	192	0xC0	x13.0
72	0x48	x5.5	200	0xC8	x13.5
80	0x50	x6.0	208	0xD0	x14.0
88	0x58	x6.5	216	0xD8	x14.5
96	0x60	x7.0	224	0xE0	x15.0
104	0x68	x7.5	232	0xE8	x15.5
112	0x70	x8.0	240	0xF0	x16.0
120	0x78	x8.5			

4.5. Integration Time

The integration (exposure) time of the YACG4C0C9SHC is controlled by the Integation time(integ_time : 0x0057, 0x0004, 0x0005) registers.

Total_integration_time = interg_time x (line_length_pck / 4)x pck_clk_period

Addr.	Register Name	Description	Default
0x0057	integ_time_hw	The integration time control [19:16]	0x00
0x0004	integ_time_h	The integration time control [15:8]	0x01
0x0005	integ_time_l	The integration time control [7:0]	0x00
0x0008	line_length_pck_h	Line Length [15:8]	0x0E
0x0009	line_length_pck_l	Line Length [7:0]	0xE0

4.6. Digital Gain Control

The digital gain processing supports both the global gain control and the separate gains control for each color channel (R, Gr, Gb, B). Each gain control register is comprised of 13bit. The bit [12:9] control the integer portion and the bit [8:0] control the decimal portion of gain (512step size). The digital gain is represented as a following equation.

$$Digital\_Gain = \left(bit[12:9] + \frac{bit[8:0]}{512} \right)$$

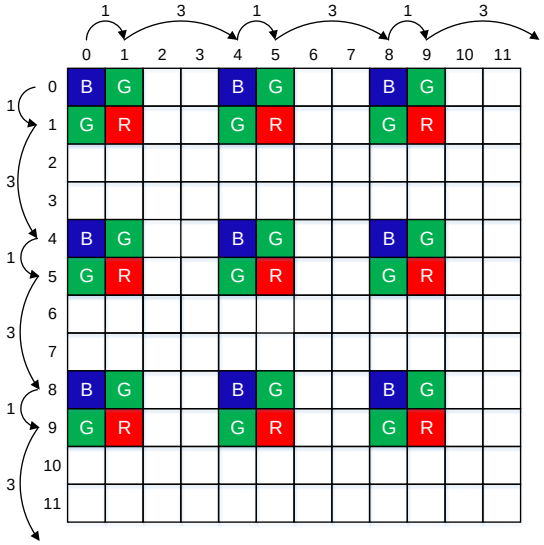
Each digital gain control register has a range from 0x through 15.99x.

4.7. Subsampling & Binning

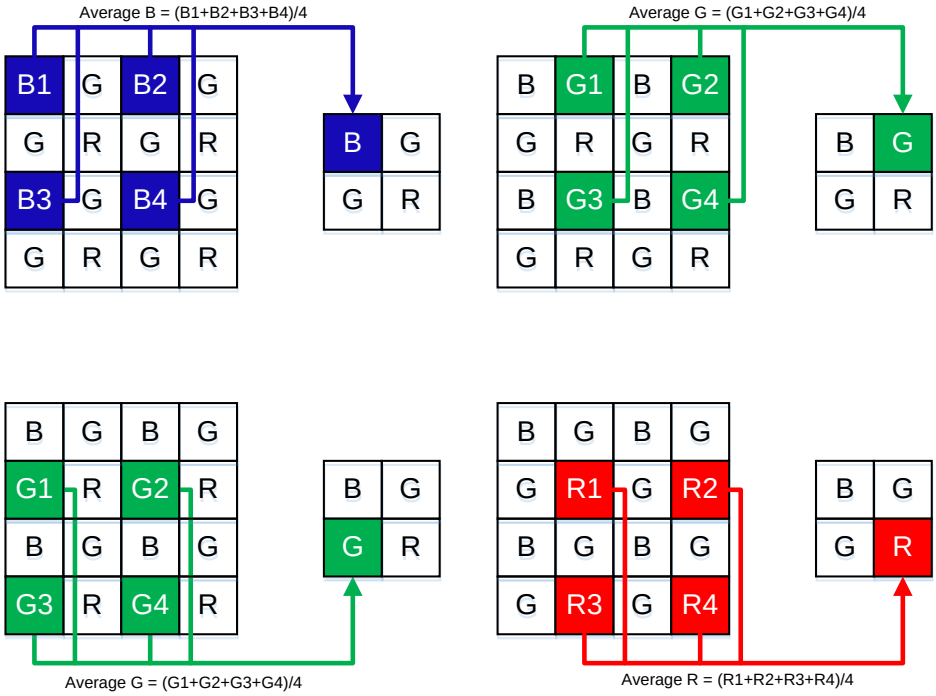
YACG4C0C9SHC supports Subsampling Mode and 2x2 Binning Mode.

Addr.	Register Name	Description	Default
0x000C	binning_mode	Binning mode enable	0x00
0x001E	x_odd_inc	Active x odd increase value	0x11
0x001F	x_even_inc	Active x even increase value	0x11
0x0032	y_odd_inc_vact	Active y odd increase value	0x11
0x0033	y_even_inc_vact	Active y even increase value	0x11

<Figure 10. 1/2 Sub Sampling mode>



<Figure 11. 2x2 Binning mode>



4.8. Horizontal Scaling

The image scaling function within a sensor module provides a downscaling operation using Bayer data to reduce the size while covering the same angle of view of the original image. Each downscaled output pixel is calculated by taking a weighted average of input pixels which are composed of neighboring pixels. The image scaling function of the Bayer Scaler supports horizontal down to x1/2 , x1/4 scale in X (Horizontal).

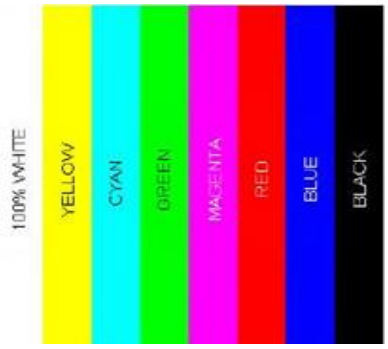
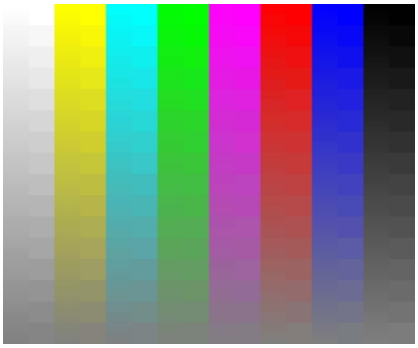
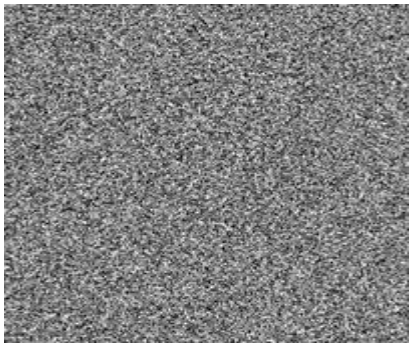
For example, when X scaling is enabled for a x1/2 scale factor, output image is reduced by half in X directions. This results in output image that is half of the input image size. The scaled output size is represented as a following equation depending on the scale factor.

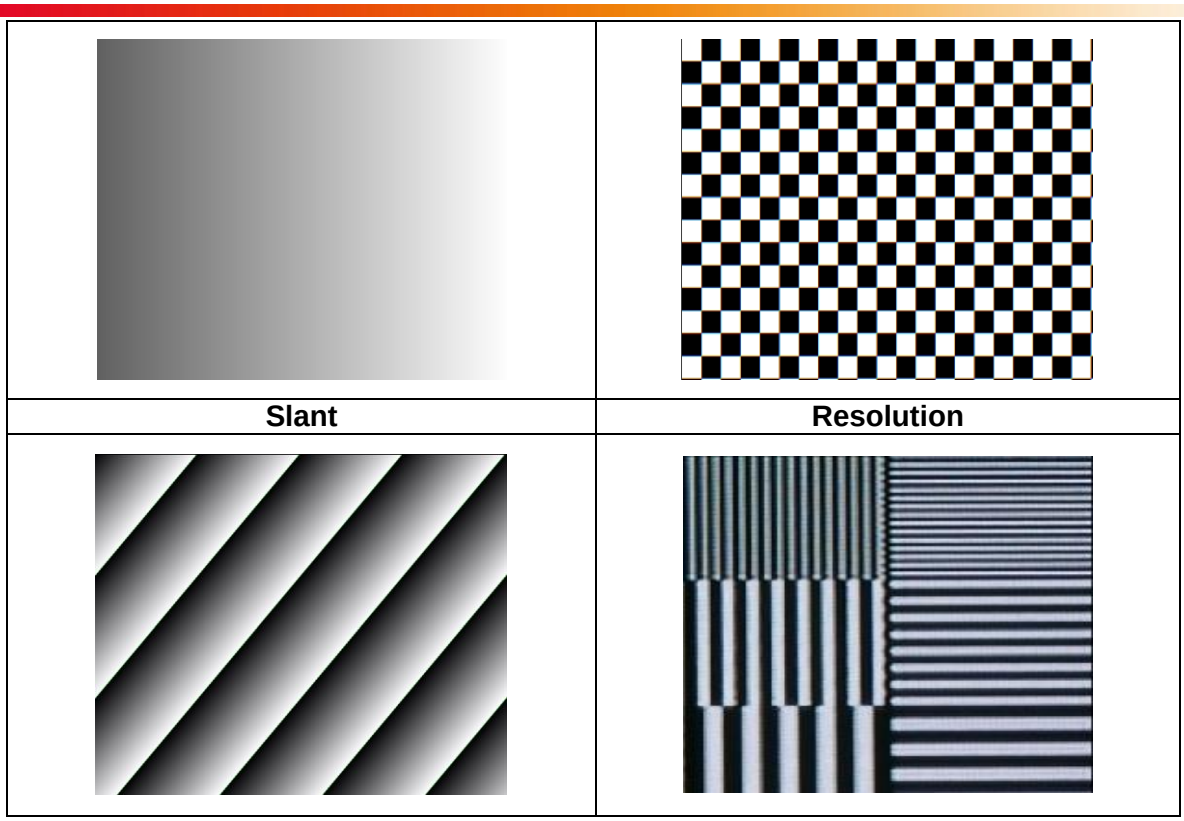
Addr.	Register Name	Description	Default
0x0A22	r_hbin_mode	Horizontal Binning Mode [2:0] : 3'h0 – Bypass [2:0] : 3'h1 – 1/2 Horizontal binning [2:0] : 3'h2 – 1/4 Horizontal binning	0x00

4.9. Test Pattern Generator

For testing, we support various test patterns, such as color bar/ fade to gray color bar/ PN9 pattern etc.

[Table 13. Test patterns]

Solid color bar	100% color bars
	
Fade to gray color bars	**PN9**
	
Horizontal/Vertical gradient	**Check board**



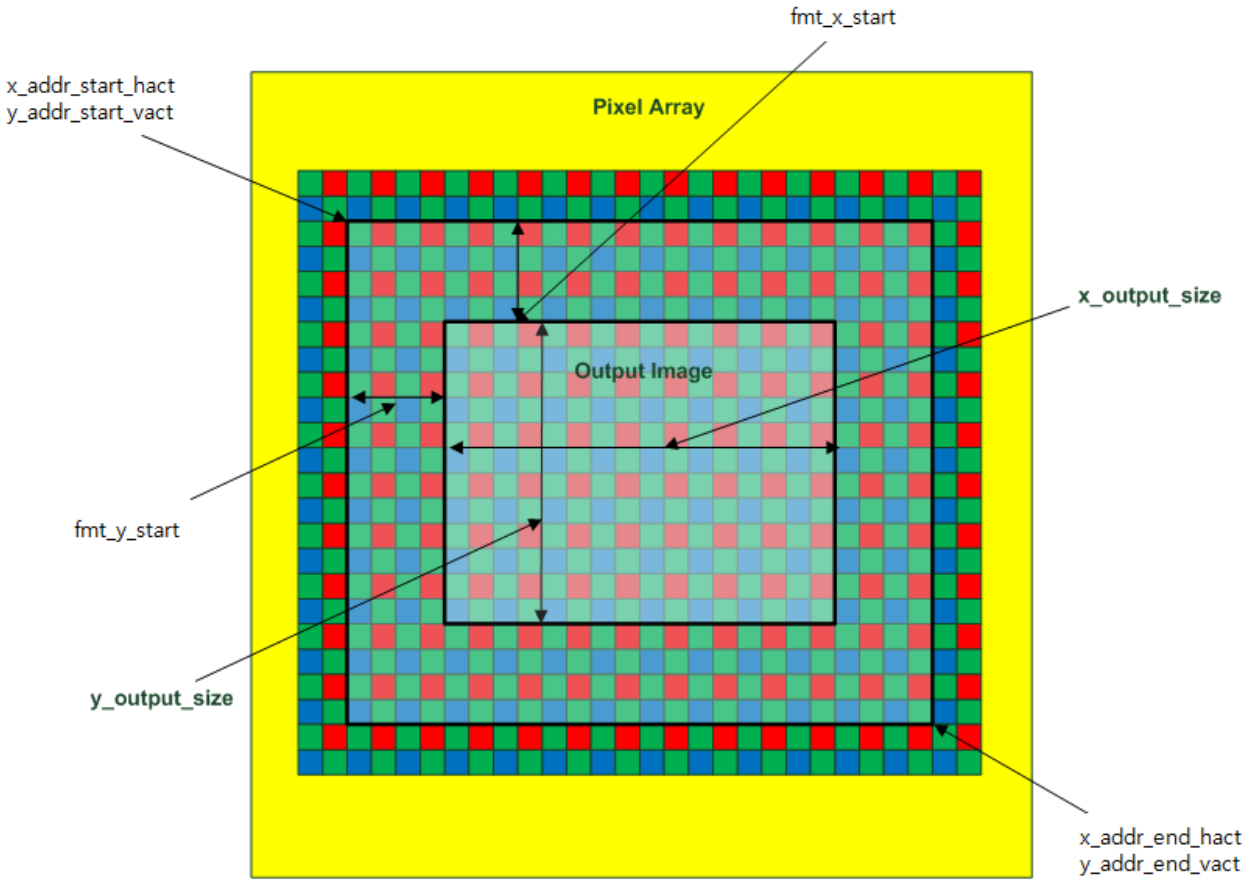
[Table 13. Test Patterns register]

Addr.	Register Name	Description	Default
0x0A05	isp_en_l	B[0] - Test pattern generation enable	0x0
0x020A	test_pattern_mode	Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – Resolution pattern 10 ~ 255 - Reserved	0x00

4.10. Windowing

Sensor has a rectangular pixel array 3264 X 2448. The array can be windowed by the output crop. These crop functions operate by controlling offset(start pixel point) register and cropping image size register.

<Figure 12. Output Image windowing >



[Table 14. Image Windowing Register]

Addr.	Register Name	Description	Default
0x0012	r_x_addr_start_hact_h	active x start address	0x00
0x0013	r_x_addr_start_hact_l		0x08
0x0026	r_y_addr_start_vact_h	active y start address	0x00
0x0027	r_y_addr_start_vact_l		0x40
0x0018	r_x_addr_end_hact_h	active x end address	0x0C
0x0019	r_x_addr_end_hact_l		0xD7
0x002C	r_y_addr_end_vact_h	active y end address	0x09
0x002D	r_y_addr_end_vact_l		0xDF

0x0A12	r_x_output_size_h	fmt column output size	0x0C
0x0A13	r_x_output_size_l		0xD0
0x0A14	r_y_output_size_h	fmt row output size	0x09
0x0A15	r_y_output_size_l		0xA0
0x0804	fmt_x_start_h	column start pixel	0x00
0x0805	fmt_x_start_l		0x00
0x0806	fmt_y_start_h	row start pixel	0x00
0x0807	fmt_y_start_l		0x00

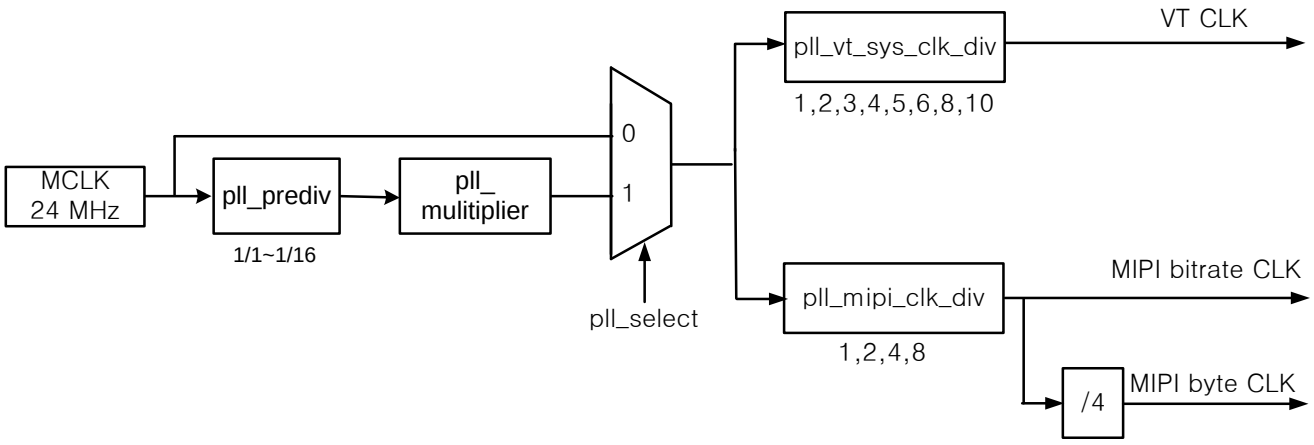
4.11. PLL

The PLL is used for clock generation for the digital block and MIPI transmitter. It consists of PFD(Phase Frequency Detector), charge pump (CP) and 2nd order loop-filter, 4-bit programmable pre-divider and 7-bit programmable multiplier. The clock generator is used for clock generation for digital part and MIPI transmitter. It consists of the divider for digital part and the divider for MIPI. The top block is shown in Figure 14

[Table 15. Register map of PLL]

Addr.	Register Name	Description	Default
0x0B16 0x0B17	pll_control1	[15] : reserved [14:8] : d2a_pll_mdiv [7:6] : d2a_pll_vt_sys_clk_div2_4 [5:2] : d2a_pll_prediv [1] : d2a_pll_reset [0] : d2a_clkgen_en	0x2D 0x0B
0x0B18 0x0B19	pll_control2	[15] : d2a_pll_clkgen_reset [14:12] : d2a_pll_vt_sys_clk_div [11] : reserved [10:8] : d2a_pll_ramp_clk_div [7:6] : d2a_pll_mipi_clk_div [5] : d2a_dcdc_clk_div [4:2] : d2a_pll_icp_sel [1] : reserved [0] : d2a_pll_clkgen_mipi_reset	0xC0 0x09

<Figure 13. Block Diagram of PLL>



4.12. MIPI

YACG4C0C9SHC supports serial data output through 1/2/4-lane MIPI(Mobile Industry Processor Interface). YACG4C0C9SHC has four data lanes and one clock lane. The MIPI output transmitter runs up to 720 Mega bit/sec each lane.

[Table 16. CSI lane mode register]

Addr.	Register Name	Description	Default
0x0902[7:6]	data_lane_mode	0x00 - 1 lane mode 0x01 - 2 lane mode 0x11 - 4 lane mode	0x11

The design follows CSI-2(Camera Serial Interface-2) specification. The CSI-2 specification defines standard data transmission and control interfaces between transmitter and receiver. The CSI-2 is unidirectional differential serial interface with data and clock signals; the physical layer of this interface is the "*MIPI Alliance Standard for D-PHY*". The high speed serial interface uses the following output-only signal pairs. (4 channnel data lanes and clock lane in accordance with CCP2 / MIPI specification.)

[Table 17. MIPI serial interface]

Output pin	Descrpition
DATA1_P / DATA1_N	Data lane Dp / Dn
DATA2_P / DATA2_N	
DATA3_P / DATA3_N	
DATA4_P / DATA4_N	
CLK_P / CLK_N	Clock lane Cp / Cn

The control interface (referred as CCI) is a bi-directional control interface compatible with I2C standard. YACG4C0C9SHC supports both continuous clock behavior and non-continuous clock behavior on the clock lane. The serial interface can reduce power consumption by entering ULPS(Ultra Low Power State) mode. Each data lanes and clock lane are set to the ULPS mode when the sensor is in the hardware standby or soft standby system state.

In order to operate MIPI serial interface, sensor must set both MIPI Power enable register and TX enable register at power up and after reset. The MIPI Reset register is used to initialize MIPI operation, normally not used.

[Table 18. Timing Configuration register]

Addr.	Register Name	Description	Default
0x0915	tlpx	D-PHY spec require : 50ns	0x05
0x0916	tclk_prepare	D-PHY spec require : > 38ns, < 95ns	0x05
0x0917	tclk_zero	D-PHY spec require : tclk_prepare + tclk_go > 300ns	0x1A
0x0919	ths_prepare	D-PHY spec require : 40ns + 4UI, < 85ns + 6UI	0x05
0x091A	ths_zero_min	D-PHY spec require : ths_prepare + ths_go > 145ns + 10UI	0x0A

0x091B	ths_trail	D-PHY spec require : > MAX(8UI, 60ns + 4UI)	0x09
0x091C	tclk_post	D-PHY spec require : > 60ns + 52UI	0x0D
0x091D	tclk_trail_min	D-PHY spec require : > 60ns	0x08

Many kinds of timing constraints are specified in the D-PHY specification. In order to satisfy this specifications, user needs to adjust timing value to control analog block. Registers from 0x0915 to 0x091D are used for this purpose. If you change the clock operating speed, reconfigulate registers.

4.13. Frame structure

Frame Structure is controlled by Line length pck, frame length lines, x_addr_start, y_addr_start, x_addr_end and y_addr_end.

Frame length lines control

1. Frame length lines are controlled by 0x0006, 0x0007 at full readout mode.

Line length pcks control

1. Line length pcks are controlled by 0x0008, 0x0009 at full/analog subsampling readout mode.
2. Minimum line length pck

-. normal,sub-sampling : 3808

Visible pixel data size control

1. Visible pixel width is controlled by x_addr_start [0x0012, 0x0013], x_addr_end [0x0018, 0x0019], y_addr_start [0x0026, 0x0027], y_addr_end[0x002C, 0x002D] when 0x0020[2], 0x0034[2] bit is enabled.

-. Visible pixel width = x_addr_end – x_addr_start + 1

-. Visible pixel height = y_addr_end – y_addr_start + 1

2. If 0x0020[2], 0x0034[2] bit is disabled , Visible pixel width and height is 0.

Blank time control

1. Line blank time

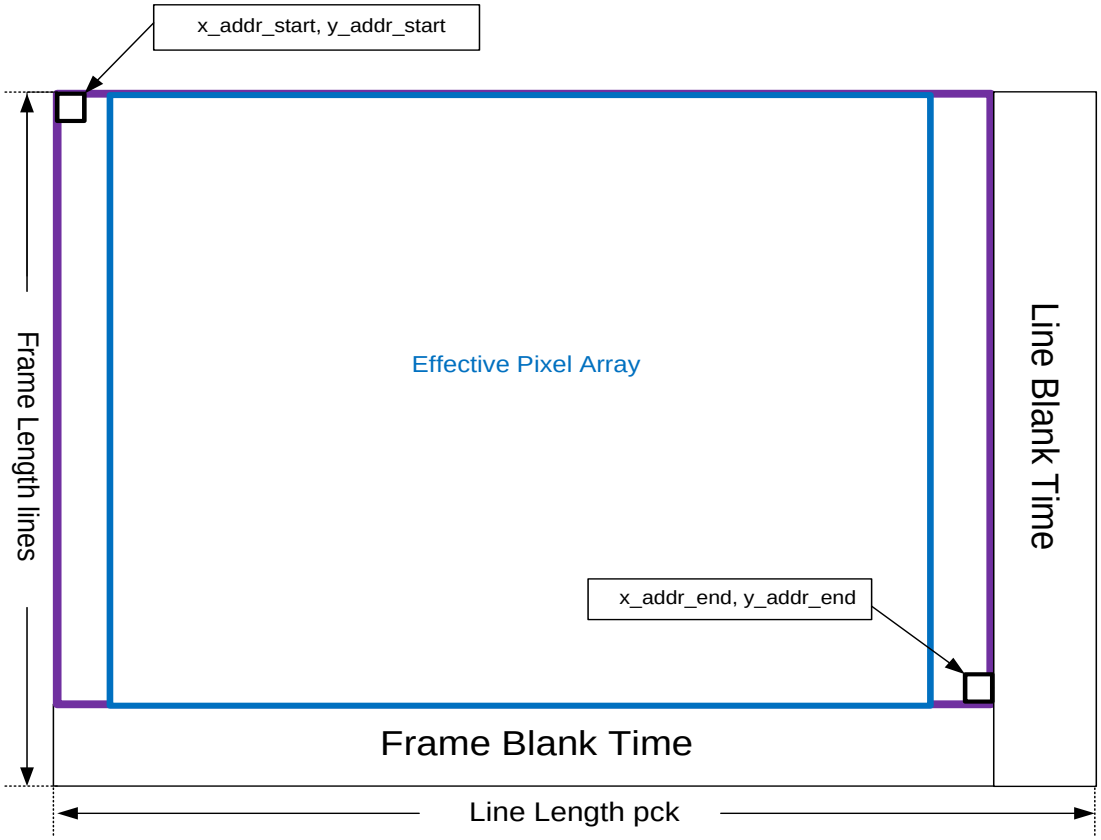
-. Line blank time = line length pck – visible pixel width

2. Frame blank time

-. Frame blank time = frame length lines – visible pixel height

-. Minimum black time : 6 lines

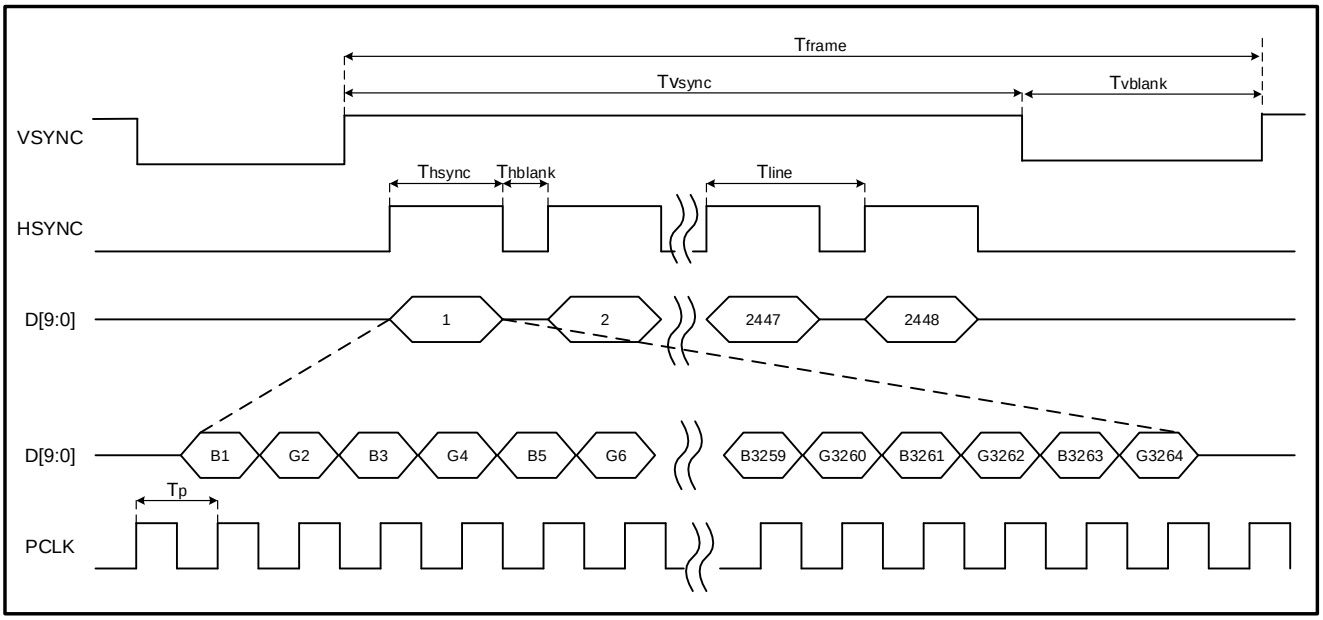
<Figure 14. Frame Structure>



4.14. Timing Description

YACG4C0C9SHC supports Croped FHD 1080P(1920x1080), HD 720P(1280x720). Following figure shows the frame timing for each image size.

<Figure 15. Frame Timing of Full Resolusion@30fps (3264 x 2448)>

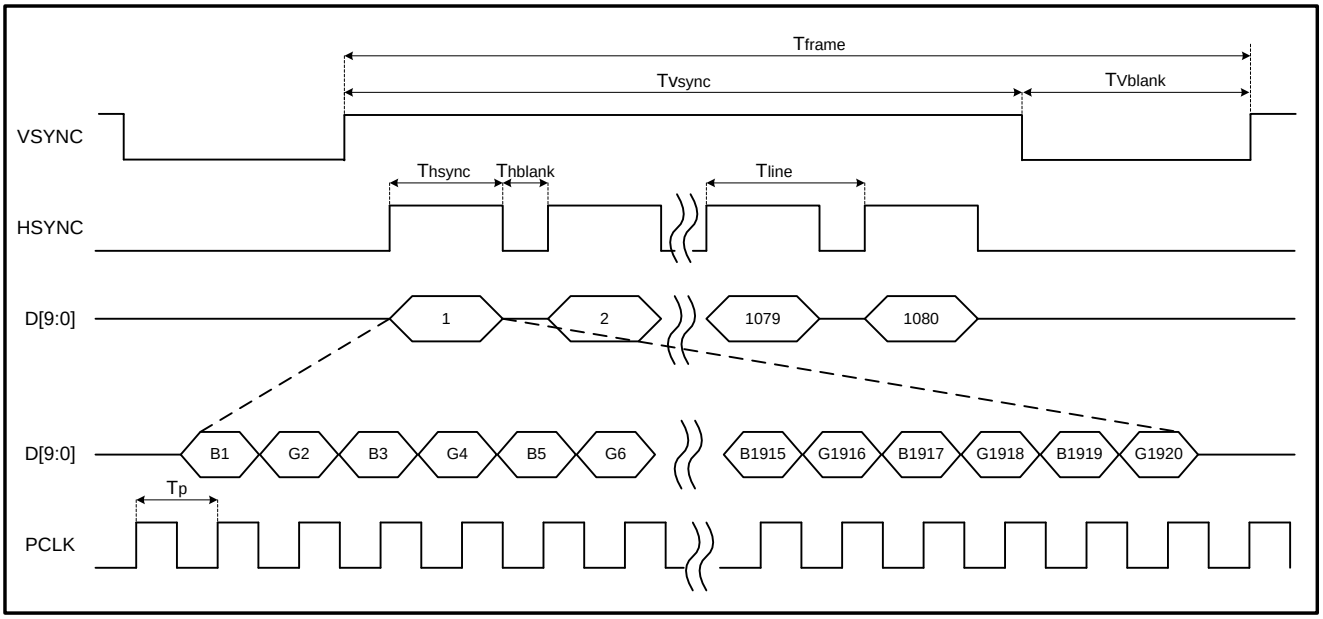


Tp = 1/8 * To

Tline = line_length_pck * To = Thsync + Thblank, Thsync = 3264 * To, Thblank = Tline - Thsync

Tframe = frame_length_lines * Tline = Tvsync + Tvblank, Tvsync = 2448 * Tline, Tvblank = Tframe – Tvsync

<Figure 16. Frame Timing of Croped FHD 1080P@60fps (1920 x 1080)>

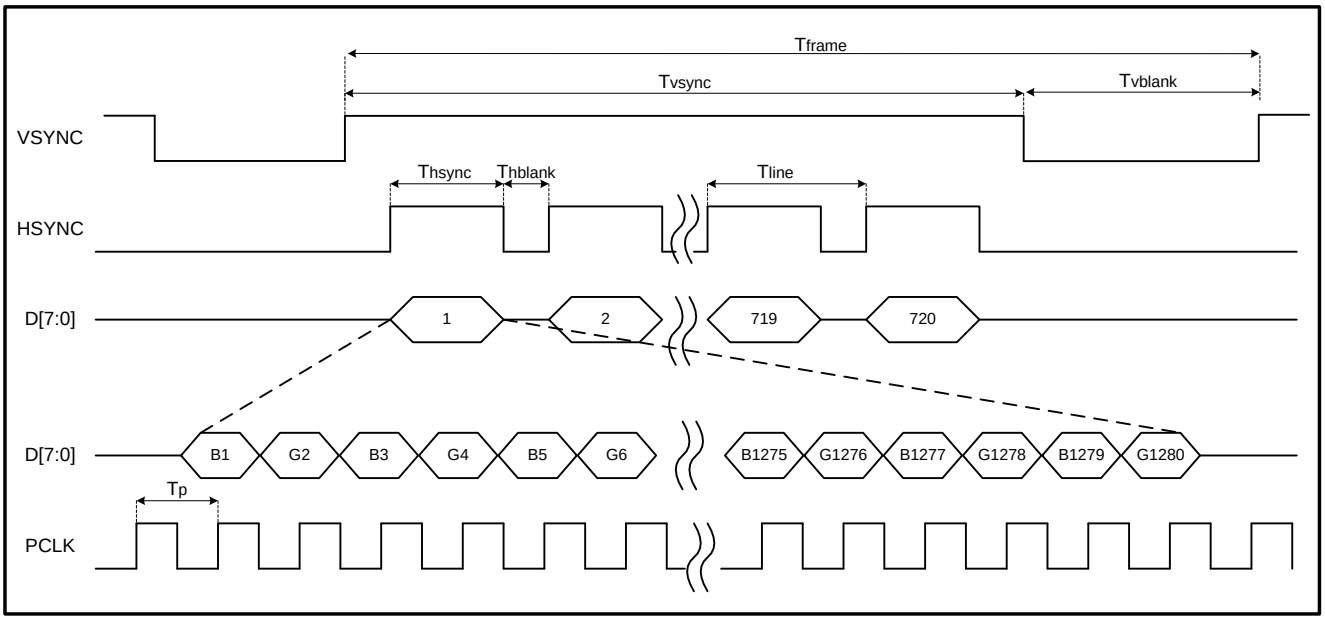


Tp = 1/8 * To

Tline = (2 * line_length_pck) * To = Thsync + Thblank, Thsync = 1920 * To, Thblank = Tline - Thsync

Tframe = (1/2 * frame_length_lines) * Tline = Tvsync + Tvblank, Tvsync = 1080 * Tline, Tvblank = Tframe - Tvsync

<Figure 17. Frame Timing of HD 720P@90fps (1280 x 720)>



Tp = 1/8 * To

Tline = (3 * line_length_pck) * To = Thsync + Thblank, Thsync = 1280 * To, Thblank = Tline - Thsync

Tframe = frame_length_lines * Tline = Tvsync + Tvblank, Tvsync = 720 * Tline, Tvblank = Tframe – Tvsync

4.15. Line-interlaced long-short output for HDR

High dynamic range (HDR) technology delivers better image quality and brighter, truer colors by accurately representing the wide range of intensity levels found in direct sunlight and in the deepest shadows.

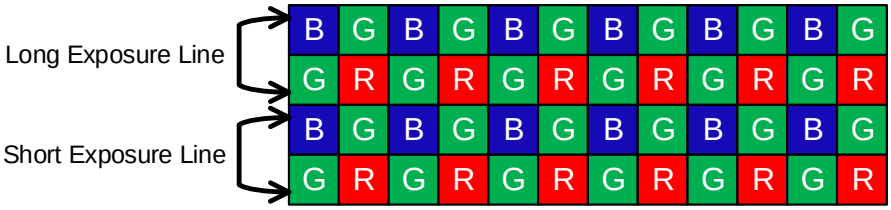
Line-interlaced long-short output for HDR, dual exposure HDR that not only improves the dynamic range, but also reduces motion artifacts and eliminates frame buffer requirements without compromising frame resolution or speed.

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into “long exposure” and “short exposure” in every two rows. Long exposure time is controlled by registers 0x0057, 0x0004 and 0x0005. Short exposure time is controlled by registers 0x0059, 0x0054 and 0x0055.

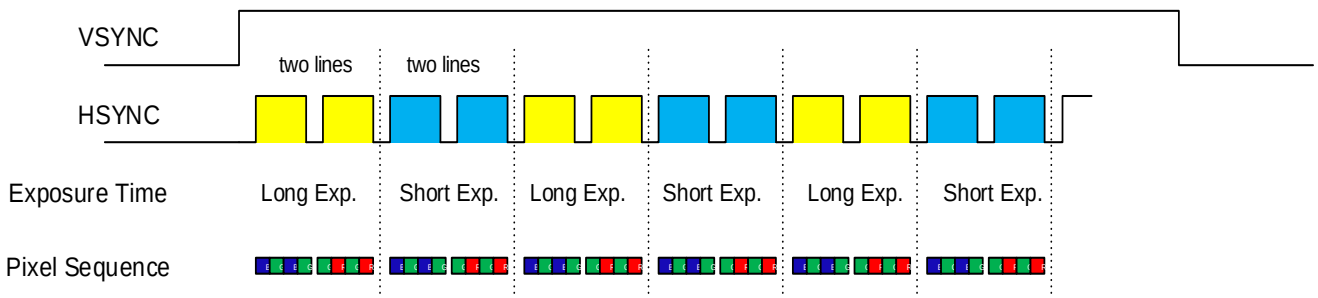
[Table 19. HDR control registers]

Addr.	Register Name	Description	Default
0x004D	hdr_en	hdr_en[0] HDR mode enable	0x00
0x0057	integ_time_hw	{ integ_time_hw[3:0], integ_time_h[8:0], integ_time_l[8:0] } → 20bit integration time for HDR mode (Long)	0x00
0x0004	integ_time_h		0x01
0x0005	integ_time_l		0x00
0x0059	integ_time_s_hw	{ integ_time_s_hw[3:0], integ_time_s_h[8:0], integ_time_s_l[8:0] } → 20bit integration time for HDR mode (Short)	0x00
0x0054	integ_time_s_h		0x01
0x0055	integ_time_s_l		0x00

<Figure 18. HDR Pixel Sequence>



<Figure 19. HDR Output Timming>



4.16. Fixed Frame Rate Timing

There are two kinds of frame rate. One is fixed frame rate and another is variable frame rate. Fixed frame rate mode can be enabled when 0x003C[0] bit is asserted. If fixed frame rate mode is enabled, maximum coarse integration time(0x0004, 0x0005) is (frame length – 6).

And variable frame rate mode can be enabled when 0x003C[0] bit is de-asserted. In variable frame rate mode, frame length is changed automatically according to coarse integration time. Specific frame length lines according to coarse integration time can be calculated by below formula.

If (coarse_integration_time < (frame_length-6))

Frame length = Register setting value of frame length lines

else

Frame length = coarse integration time + 6

And frame time can be calculated by below formula.

Frame time = (line length pck) x (frame length) x VT_CLK_priode.

[Table 20. Frame Time Calculation]

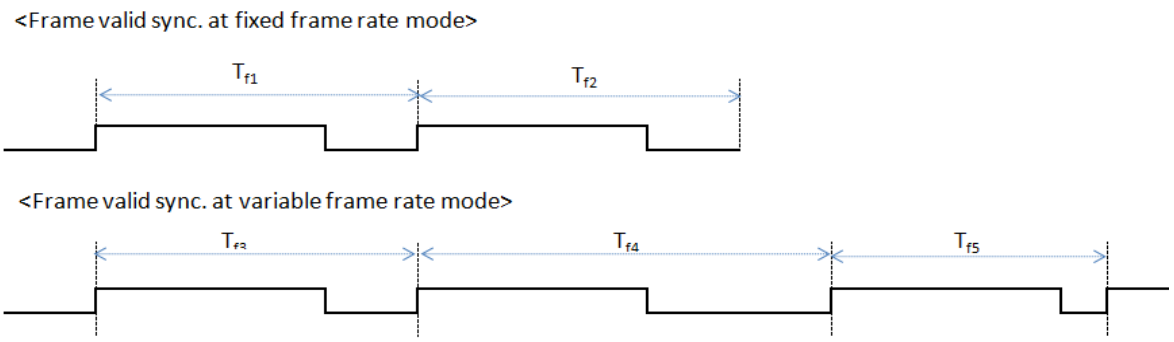
Fixed Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = 6
Else if (Coarse_Integration_Time > Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Coarse_Integration_Time = Frame_Length - 6
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time

Variable Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = Min_Coarse_Integration_Time
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time
 	
If (Coarse_Integration_Time ≤ Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Frame_Length = Frame_Length
Else
➔ Frame_Length = Coarse_Integration_Time + 6(Coarse_Integration_Time _Max_Margin)

<Figure 20. Timing of Fixed Frame Rate>



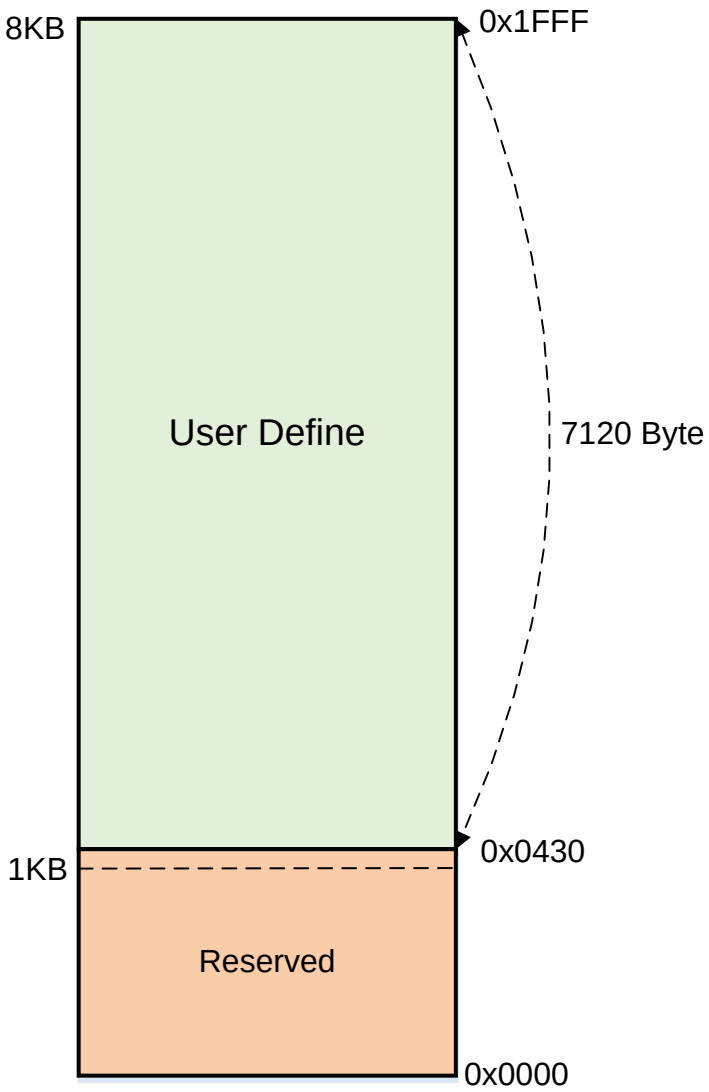
4.17. OTP Memory Map

The YACG4C0C9SHC features 8KByte of OTP (one time programmable) memory for storing ADPC data, individual moduel and sensor specific information. The user may program which set to be used. OTPM can be accessed via two-wire serial interface.

If user want to get more information, please contact to SKhynix FAE engineer or refer to sererate OTP guide documents.

Figure 22 shows the OTP Memory Map.

<Figure 21. OTP Memory Map>



5. REGISTER DESCRIPTION

[Table 21. Register Description]

sensor address in two-wire serial bus : 40H(write) , 41H(read) RO[read only]

Address (Hex)	Register	Description	Default (Hex)	Renewal Frame
		TG Registers		
0x0000	image_orient	Image orientation	0x00	Next
0x0004	coarse_integ_time	The integration time control { integ_time_hw[3:0], integ_time_h [8:0], integ_time_l [8:0] } → 20bit @integration time for HDR mode (Long)	0x01	Next
0x0005			0x00	Next
0x0006	frame_length_lines	Frame Length	0x09	Next
0x0007			0xD8	Next
0x0008	line_length_pck	Line Length	0x0E	Next
0x0009			0xE0	Next
0x000C	binning_mode	Binning mode enable	0x00	Next
0x0012	x_addr_start	active x start address	0x00	Next
0x0013			0x08	Next
0x0018	x_addr_end	active x end address	0x0C	Next
0x0019			0xD7	Next
0x001E	x_odd_inc	Active x odd increase value	0x11	Next
0x001F	x_even_inc	Active x even increase value	0x11	Next
0x0026	y_addr_start	active y start address	0x00	Next
0x0027			0x40	Next
0x002C	y_addr_endt	active y end address	0x09	Next
0x002D			0xDF	Next
0x002E	y_odd_inc_fobp	Frame obp y odd increase value	0x11	Next
0x002F	y_even_inc_fobp	Frame obp y even increase value	0x11	Next
0x0032	y_odd_inc_vact	Active y odd increase value	0x11	Next
0x0033	y_even_inc_vact	Active y even increase value	0x11	Next
0x003B	analog_gain_code_global	Analog Gain	0x00	Next
0x0046	r_grouped_para_hold	Grouped parameter hold	0x00	Next
0x004C	tg_enable	TG enable	0x00	Current
0x004D	hdr_en	HDR mode enable	0x00	Next
0x0057	integ_time_hw	integ_time_hw[3:0] @integration time for HDR mode (Long)	0x00	Next
0x0059	integ_time_s_hw	{ integ_time_s_hw[3:0], integ_time_s_h[8:0], integ_time_s_l[8:0] } → 20bit	0x00	Next
0x0054	integ_time_s_h		0x01	Next
0x0055	integ_time_s_l	integration time for HDR mode (Short)	0x00	Next

OTP Registers				
0x0102	otp_cmd	OTP command for read/write	0x00	Current
0x0106	otp_wdata	OTP write data	0x00	Current
0x0108	otp_rdata	OTP read data	0x00	Current
0x010A	otp_addr	OTP write/read address	0x00	Current
0x010B			0x00	Current
Test Pattern Registers				
0x020A	test_pattern_mode	Test Pattern mode	0x00	Next
0x020C	test_data_red	The test data used to replace red pixel data	0x00	Next
0x020D			0x00	Next
0x020E	test_data_greenR	The test data used to replace green pixel data on rows that also have red pixels	0x00	Next
0x020F			0x00	Next
0x0210	test_data_blue	The test data used to replaced blue pixel data	0x00	Next
0x0211			0x00	Next
0x0212	tetst_data_greenB	The test data used to replaced green pixel data on rows that also have blue pixels	0x00	Next
0x0213			0x00	Next
0x0214	horizontal_cursor_width	Defines the width of the horizontal cursor(in pixels)	0x00	Next
0x0215			0x00	Next
0x0216	horizontal_cursor_position	Defines the top edge of the horizontal cursor	0x00	Next
0x0217			0x00	Next
0x0218	vertical_cursor_width	Defines the width of the vertical cursor(in pixels)	0x00	Next
0x0219			0x00	Next
0x021A	vertical_cursor_position	Defines the left hand edge of the vertical cursor. A value of 0xFFFF switches the vertical cursor into automatic mode where it automatic mode where it automatically advances every frame.	0x00	Next
0x021B			0x00	Next
Digital Gain Registers				
0x0508	dgain_gr	Digital Gr gain control (0 ~ 15.99x)	0x02	Next
0x0509			0x00	Next
0x050A	dgain_gb	Digital Gb gain control (0 ~ 15.99x)	0x02	Next
0x050B			0x00	Next
0x050C	dgain_r	Digital R gain control (0 ~ 15.99x)	0x02	Next
0x050D			0x00	Next
0x050E	dgain_b	Digital B gain control (0 ~ 15.99x)	0x02	Next
0x050F			0x00	Next
Formatter Control Registers				
0x0804	x_start_h	column start pixel (high byte)	0x00	Next
0x0805	x_start_l	column start pixel (low byte)	0x00	Next
0x0806	y_start_h	row start pixel (high byte)	0x00	Next

0x0807	y_start_l	row start pixel (low byte)	0x00	Next
MIPI Control Registers				
0x0902	MIPI_tx_op_mode	MIPI operating mode	0xC3	Current
0x0915	tlpx	length of any Low-Power state period.	0x05	Current
0x0916	tclk_prepare	time to drive LP-00 to prepare for HS clock transmission	0x05	Current
0x0917	tclk_zero	time for lead HS-0 drive period before starting clock.zero	0x1A	Current
0x0919	ths_prepare	time to drive LP-00 before starting the HS transmission on a Data Lane.	0x05	Current
0x091A	ths_zero	time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.	0x0A	Current
0x091B	ths_trail	time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst.	0x09	Current
0x091C	tclk_post	time that the transmitter	0x0D	Current
0x091D	tclk_trail_min	the time to drive HS differential state after last layload clock bit of a HS transmission burst.	0x08	Current
ISP Common Registers				
0x0A00	mode_sel	streaming mode	0x00	Current
0x0A02	fast_standby_mode	fast standby mode	0x00	Current
0x0A04	isp_en	Isp enable	0x01	Current
0x0A05			0x40	Current
0x0A10	data_pedestal	data pedestal value	0x40	Current
0x0A1A	pedestal_en	Pedestal enable	0x00	Current
Window Registers				
0x0A12	x_output_size	Formatter column output size	0x0C	Next
0x0A13			0xD0	Next
0x0A14	y_output_size	Formatter row output size	0x09	Next
0x0A15			0xA0	Next
Horizontal Scale Register				
0x0A22	hbin_mode	Horizontal Scale Mode	0x00	Next
BLC Control Registers				
0x0C00	blc_ctl1	BLC enable	0x8C	Current
PAD Control				
0x0D00	drvst_fsync	driving strength of FSYNC IO.	0x07	Current
0x0D01	drvst_sda	driving strength of SDA	0x07	Current
0x0D02	drvst_strobe	driving strength of STROBE	0x07	Current
System Control Registers				
0x0F02	pll_cfg1	pll enable	0x00	Current
0x0F03	pll_cfg2	pll_lock_time control	0x06	Current
0x0F14	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0x20	Current
0x0F16	model_id_lo	mode ID low byte	0x43	RO

0x0F17	model_id_hi	model ID high byte	0x08	RO

5.1. TG Control Registers

0x0000: image_orientation [default=0x00, r/w]

Bit	Function	Description	Default
B[7:2]		Reserved	0000_00b
B[1]	V_flip	Vertical Flip Enable [0: no flip, 1: Vertical Flip]	0b
B[0]	H_mirror	Horizontal Mirror Enable [0:no mirror,1:Horizontal Mirror]	0b

0x0004: coarse_integration_time_h [default=0x01, r/w]

Bit	Function	Description	Default
B[7:0]	coarse_integration_time_h	The coarse integration time control	0000_0001b

0x0005: coarse_integration_time_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	coarse_integration_time_l	The coarse integration time control	0000_0000b

0x0006: frame_length_lines_h [default=0x09, r/w]

Bit	Function	Description	Default
B[7:0]	frame_length_lines_h	Frame length (Units : lines)	0000_1001b

0x0007: frame_length_lines_l [default=0xD8, r/w]

Bit	Function	Description	Default
B[7:0]	frame_length_lines_l	Frame length (Units : lines)	1101_1000b

0x0008: line_length_pck_h [default=0x0E, r/w]

Bit	Function	Description	Default
B[7:0]	frame_length_lines_h	Frame length (Units : lines)	0000_1110b

0x0009: line_length_pck_l [default=0xE0, r/w]

Bit	Function	Description	Default
B[7:0]	frame_length_lines_l	Frame length (Units : lines)	1110_0000b

0x000C: binning_mode [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	binning_mode	0 - None 1 - enabled	0b

0x0012: x_addr_start_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	x_addr_start_h	x start address	0000_0000b

0x0013: x_addr_start_l [default=0x08, r/w]

Bit	Function	Description	Default
B[7:0]	x_addr_start_l	x start address	0000_1000b

0x0018: x_addr_ end _h [default=0x0C, r/w]

Bit	Function	Description	Default
B[7:0]	x_addr_ end_h	x end address	0000_1100b

0x0019: x_addr_end_l [default=0xD7, r/w]

Bit	Function	Description	Default
B[7:0]	x_addr_ end_l	x end address	1101_0111b

0x001E: x_odd_inc [default=0x11, r/w]

Bit	Function	Description	Default
B[7:0]	x_odd_inc	Increment for odd pixels in the readout order	0001_0001b

0x001F: x_even_inc [default=0x01, r/w]

Bit	Function	Description	Default
B[7:0]	x_even_inc	Increment for even pixels in the readout order	0001_0001b

0x0026: y_addr_start_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	y_addr_start_h	y start address	0000_0000b

0x0027: y_addr_start_l [default=0x40, r/w]

Bit	Function	Description	Default
B[7:0]	y_addr_start_l	y start address	0100_0000b

0x002C: y_addr_ end _h [default=0x09, r/w]

Bit	Function	Description	Default
B[7:0]	y_addr_ end_h	y end address	0000_1001b

0x002D: y_addr_end_l [default=0xDF, r/w]

Bit	Function	Description	Default
B[7:0]	y_addr_ end_l	y end address	1101_1111b

0x002E: y_odd_inc_fobp [default=0x11, r/w]

Bit	Function	Description	Default
B[7:0]	y_odd_inc_fobp	Increment for frame obp odd lines in the readout order	0001_0001b

0x002F: y_even_inc_fobp [default=0x11, r/w]

Bit	Function	Description	Default
B[7:0]	y_evne_inc_fobp	Increment for frame obp odd lines in the readout order	0001_0001b

0x0032: y_odd_inc_vact [default=0x11, r/w]

Bit	Function	Description	Default
B[7:0]	y_odd_inc _vact	Increment for odd lines in the readout order	0001_0001b

0x0033: y_even_inc_vact [default=0x11, r/w]

Bit	Function	Description	Default
B[7:0]	y_even_ inc_vact	Increment for even lines in the readout order	0001_0001b

0x003B: analog_gain_code_global [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Analog_gain_code_global	Global Analogue Gain Code	0000_0000b

0x0046: grouped_para_hold [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	grouped_para_hold	grouped parameter hold Set to envelope a series of parameter changes as a group of changes that should be made so as to effect the output stream on the same frame boundary	0b

0x004C: tg_enable [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	tg_enable	0 : tg_disable 1 : tg_enable	0b

0x004D: hdr_en [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	hdr_en	0 : HDR Mode disable 1 : HDR Mode enable	0b

0x0054: integration_time_s_h [default=0x01, r/w]

Bit	Function	Description	Default
B[7:0]	integration_time_s_h	The integration time for HDR mode (Short) – < Related reg. 0x0059, 0x0055 >	0000_0001b

0x0055: integration_time_s_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	integration_time_s_l	The integration time for HDR mode(Short) - < Related reg. 0x0059, 0x0054 >	0000_0000b

0x0057: integration_time_hw [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	integration_time_hw	The integration time control < Related reg. 0x0004, 0x0005 >	0000_0000b

0x0059: integration_time_s_hw [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	integration_time_s_hw	The integration time for HDR mode (Short) < Related reg. 0x0054, 0x0055 >	0000_0000b

5.2. OTP

0x0102: otp_cmd [default=0x00, r/w]

Bit	Function	Description	Default
B[7:2]		Reserved	0000_00b
B[1]	otp_write_cmd	Continuous write	0b
B[0]	otp_read_cmd	Continuous read	0b

0x0106: otp_wdata [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_wdata	OTP write data	0000_0000b

0x0108: otp_rdata [default=0x00, r/o]

Bit	Function	Description	Default
B[7:0]	otp_rdata	OTP read data	0000_0000b

0x010A: otp_addr_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_addr_h	OTP write/read address high	0000_0000b

0x010B: otp_addr_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_addr_l	OTP write/read address low	0000_0000b

5.3. TPG

0x020A: test_pattern_mode [default=0x00, r/w]

Bit	Function	Description	Default
B[7:4]		Reserved	0000b
B[3:0]	Test_pattern _mode	Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – resolution pattern 10 ~ 255 - Reserved	0000b

0x020C: test_data_red_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_red _h	The test data used to replace red pixel data (high byte [15:8])	0000_0000b

0x020D: test_data_red_l [default=0x0A, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_red _l	The test data used to replace red pixel data (low byte [7:0])	0000_0000b

0x020E: test_data_greenR_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_gre enR_h	The test data used to replace greenR pixel data (high byte [15:8])	0000_0000b

0x020F: test_data_ greenR_l [default=0x0A, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_ greenR_l	The test data used to replace greenR pixel data (low byte [7:0])	0000_0000b

0x0210: test_data_blue_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_blue _h	The test data used to replace blue pixel data (high byte [15:8])	0000_0000b

0x0211: test_data_blue_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_blue _l	The test data used to replace blue pixel data (low byte [7:0])	0000_0000b

0x0212: test_data_greenB_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_gre enB_h	The test data used to replace greenB pixel data (high byte [15:8])	0000_0000b

0x0213: test_data_greenB_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	test_data_gre enB_l	The test data used to replace greenB pixel data (low byte [7:0])	0000_0000b

0x0214: horizontal_cursor_width_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Horizontal_cursor_width_h	Defines the width of the horizontal cursor(in pixels) (high byte [15:8])	0000_0000b

0x0215: horizontal_cursor_width_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Horizontal_cursor_width_l	Defines the width of the horizontal cursor(in pixels) (low byte [7:0])	0000_0000b

0x0216: horizontal_cursor_position_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Horizontal_cursor_position_h	Defines the top edge of the horizontal cursor (high byte [15:8])	0000_0000b

0x0217: horizontal_cursor_position_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Horizontal_cursor_position_l	Defines the top edge of the horizontal cursor (low byte [7:0])	0000_0000b

0x0218: vertical_cursor_width_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Vertical_cursor_width_h	Defines the width of the vertical cursor(in pixels) (high byte [15:8])	0000_0000b

0x0219: vertical_cursor_width_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Vertical_cursor_width_l	Defines the width of the vertical cursor(in pixels) (low byte [7:0])	0000_0000b

0x021A: vertical_cursor_position_h [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Vertical_cursor_position_h	Defines the left hand edge of the vertical cursor. (high byte [15:8]) A value of 0xFFFF switches the vertical cursor into automatic mode where it automatic mode where it automatically advances every frame.	0000_0000b

0x021B: vertical_cursor_position_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Vertical_cursor_position_l	Defines the left hand edge of the vertical cursor. (low byte [7:0]) A value of 0xFFFF switches the vertical cursor into automatic mode where it automatic mode where it automatically advances every frame.	0000_0000b

5.4. Digital Gain

0x0508: digital_gain_gr_h [default=0x02, r/w]

Bit	Function	Description	Default
B[7:5]	digital_gain_gr_h	Reserved	000b
B[4:0]		Digital gain for Gr channel (high byte [12:8])	0_0010b

0x0509: digital_gain_gr_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	digital_gain_gr_l	Digital gain for Gr channel (low byte [7:0])	0000_0000b

0x050A: digital_gain_gb_h [default=0x02, r/w]

Bit	Function	Description	Default
B[7:5]	Digital_gain_greenB	Reserved	000b
B[4:0]		Digital gain for Gb channel (high byte [12:8])	0_0010b

0x050B: digital_gain_gb_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Digital_gain_gb_l	Digital gain for Gb channel (low byte [7:0])	0000_0000b

0x050C: digital_gain_r_h [default=0x02, r/w]

Bit	Function	Description	Default
B[7:5]	Digital_gain_r_h	Reserved	000b
B[4:0]		Digital gain for R channel (high byte [12:8])	0_0010b

0x050D: digital_gain_r_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Digital_gain_r_l	Digital gain for R channel (low byte [7:0])	0000_0000b

0x050E: digital_gain_b_h [default=0x02, r/w]

Bit	Function	Description	Default
B[7:5]	Digital_gain_b_h	Reserved	000b
B[4:0]		Digital gain for B channel (high byte [12:8])	0_0010b

0x050F: digital_gain_b_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Digital_gain_b_l	Digital gain for B channel (low byte [7:0])	0000_0000b

5.6. FORMATTER

0x0804: X_START_H [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	X_START_H	Column start pixel	0000_0000b

0x0805: X_START_L [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	X_START_L	Column start pixel	0000_0000b

0x0806: Y_START_H [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Y_START_H	Row start pixel	0000_0000b

0x0807: Y_START_L [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	Y_START_L	Row start pixel	0000_0000b

5.7. MIPI

0x0902:MIPI_tx_op_mode [default=0xC3, r/w]

Bit	Function	Description	Default
B[7:6]	Lane Mode	MIPI lane mode 00 : 1 lane mode 01 : 2 lane mode 11 : 4 lane mode	11b
B[5]	Data Format	MIPI data format 0 : RAW10 mode 1 : RAW8 mode	0b
B[4]	Line synchronization	Line synchronization enable 1 : MIPI line start/end pachet on 0 : MIPI line start/end packet off	0b
B[3]	MIPI line number	MIPI line number enable 1 : MIPI line number on 0 : MIPI line number off	0b
B[2]	MIPI frame number	MIPI frame number enable 1 : MIPI frame number on 0 : MIPI frame number off	0b
B[1]	MIPI clock mode	MIPI clock mode selection 0:non-continuous clock mode 1:continuous clock mode	1b
B[0]	MIPI frame number	MIPI frame count reset 0 : MIPI frame count reset off 1 : MIPI frame count reset on	1b

0x0915: tlpx [default=0x05, r/w]

Bit	Function	Description	Default
B[7:0]	Tlpx	Tlpx is the length of any Low-Power state period	0000_0101b

0x0916: tclk_prepare [default=0x05, r/w]

Bit	Function	Description	Default
B[7:0]	Tclk_prepare	Tclk prepare is the time to drive LP-00 to prepare for HS clock transmission.	0000_0101b

0x0917: tclk_zero [default=0x1A, r/w]

Bit	Function	Description	Default
B[7:0]	Tclk_zero	Tclk zero is the time for lead HS-0 drive period before starting clock	0001_1010b

0x0919: ths_prepare [default=0x05, r/w]

Bit	Function	Description	Default
B[7:0]	Ths_prepare	Ths prepare is the time to drive LP-00 before starting the HS transmission on a Data Lane.	0000_0101b

0x091A: ths_zero [default=0x0A, r/w]

Bit	Function	Description	Default
B[7:0]	Ths_zero	Ths zero minimum is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence	0000_1010b

0x091B: ths_trail [default=0x09, r/w]

Bit	Function	Description	Default
B[7:0]	Ths_trail	Ths trail is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.	0000_1001b

0x091C: tclk_post [default=0x0D, r/w]

Bit	Function	Description	Default
B[7:0]	Tclk_post	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode. Host will control that suitable value is used	0000_1101b

0x091D: tclk_trail_min [default=0x08, r/w]

Bit	Function	Description	Default
B[7:0]	Tclk_trail_min	Tclk trail minimum is the time to drive HS differential state after last layload clock bit of a HS transmission burst.	0000_1000b

5.8. ISP Common

0x0A00: mode_sel [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	mode_sel	1 – streaming 0 – sw_standby	0b

0x0A02: fast_standby_mode [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	fast_standby_ mode	1 – fast standby mode (enable mode change from streaming mode to sw standby mode at line blank) 0 – sw_standby	0b

0x0A04: isp_en_h [default=0x01, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	mipi enable	MIPI enable	1b

0x0A05: isp_en_l [default=0x40, r/w]

Bit	Function	Description	Default
B[7]		Reserved	0b
B[6]	fmt enable	Formatter enable	1b
B[5]	H scaler enable	Horizontal scaler enable	0b
B[4]		Reserved	0b
B[3]	dga enable	Digital gain enable	0b
B[2]	lsc enable	Lens shading correction enable	0b
B[1]	adpc enable	adpc enable	0b
B[0]	tpg enable	Test pattern generation enable	0b

0x0A10: data_pedestal [default=0x40, r/w]

Bit	Function	Description	Default
B[7:0]	data_pedestal	data pedestal value	0100_0000b

0x0A1A: pedestal_en [default=0x00, r/w]

Bit	Function	Description	Default
B[7:4]		Reserved	0000b
B[3]	Pedestal_en	DGA Pedestal enble	0b
B[2:0]		Reserved	000b

5.9. Window

0x0A12: x_output_size_h [default=0x0C, r/w]

Bit	Function	Description	Default
B[7:0]	x_output_size_h	Formatter column output size (MSB)	0000_1100b

0x0A13: x_output_size_l [default=0xD0, r/w]

Bit	Function	Description	Default
B[7:0]	x_output_size_l	Formatter column output size (LSB)	1101_0000b

0x0A14: y_output_size_h [default=0x09, r/w]

Bit	Function	Description	Default
B[7:0]	y_output_size_h	Formatter row output size (MSB)	0000_1001b

0x0A15: y_output_size_l [default=0xA0, r/w]

Bit	Function	Description	Default
B[7:0]	y_output_size_l	Formatter row output size (LSB)	1010_0000b

5.10. Horizontal SCALER

0x0A22: hbin_mode [default=0x00, r/w]

Bit	Function	Description	Default
B[7:3]		Reserved	0000_0b
B[2:0]	X Scale Ratio	Downscale ratio of X dimension 3'h4 : 1/8 scale 4'h2 : 1/4 scale 4'h1 : 1/2 scale 4'h0 : Bypass	000b

5.11. BLC

0x0C00: blc_ctl0 [default=0x8C, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	1000_110b
B[0]	en_blc	BLC enable	0b

5.12. PAD CTRL

0x0D00: drvst_fsync [default=0x07, r/w]

Bit	Function	Description	Default
B[7:3]		Reserved	0000_0b
B[2:0]	drvst_fsync	driving strength of FSYNC IO.	111b

0x0D01: drvst_sda [default=0x07, r/w]

Bit	Function	Description	Default
B[7:3]		Reserved	0000_0b
B[2:0]	drvst_sda	driving strength of SDA	111b

0x0D02: drvst_strobe [default=0x07, r/w]

Bit	Function	Description	Default
B[7:3]		Reserved	0000_0b
B[2:0]	drvst_strobe	driving strength of STROBE	111b

5.13. SMU

0x0F02: pll_cfg1 [default=0x00, r/w]

Bit	Function	Description	Default
B[7:1]		Reserved	0000_000b
B[0]	pll_cfg1	0 – pll bypass 1 – pll enable	0b

0x0F03: pll_cfg2 [default=0x06, r/w]

Bit	Function	Description	Default
B[7:0]	pll_cfg2	pll lock time = pll_cfg2[7:0] * 256 cycle * MCLK period	0000_0110b

0x0F14: sensor_id [default=0x20, r/w]

Bit	Function	Description	Default
B[7:0]	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0010_0000b

0x0F16: model_id_l [default=0x43, r/o]

Bit	Function	Description	Default
B[7:0]	model_id_l	Sensor model ID lower byte	0100_0011b

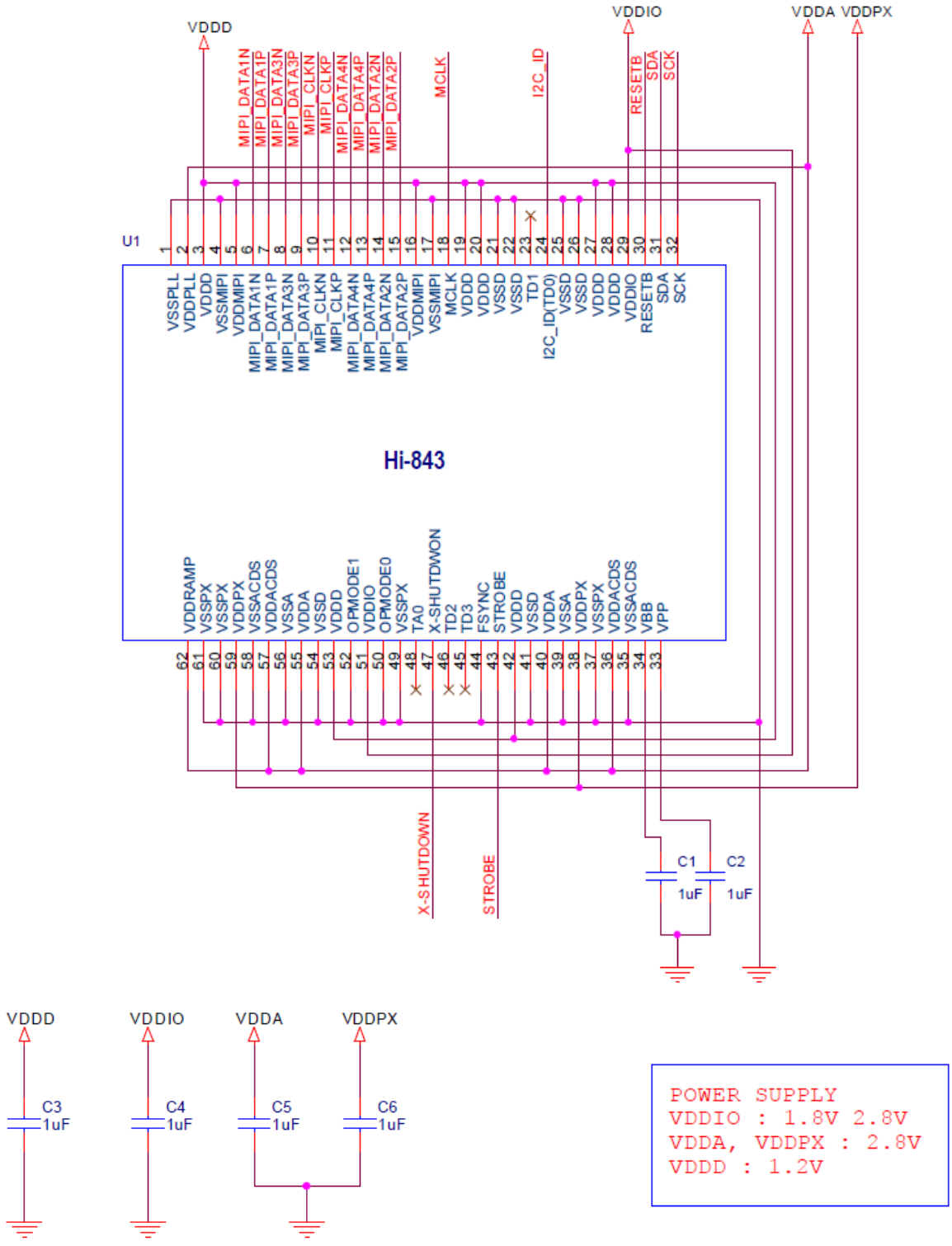
0x0F17: model_id_h [default=0x08, r/o]

Bit	Function	Description	Default
B[7:0]	model_id_h	Sensor model ID higher byte	0000_1000b

6. Reference Module Schematic

6.1. MIPI Pixel Data Interface

<Figure 22. Module Schematic>



POWER SUPPLY
VDDIO : 1.8V 2.8V
VDDA, VDDPX : 2.8V
VDDD : 1.2V

I2C Slave Address Select

PAD #24(I2C_ID) Input Low(GND)	0x40 @8bit
PAD #24(I2C_ID) Input High(VDDIO)	0xC0 @8bit

For more stable working, recommend that DGND and AGND are tied.

7. Spectral Response

<Figure 23. Spectral Response>